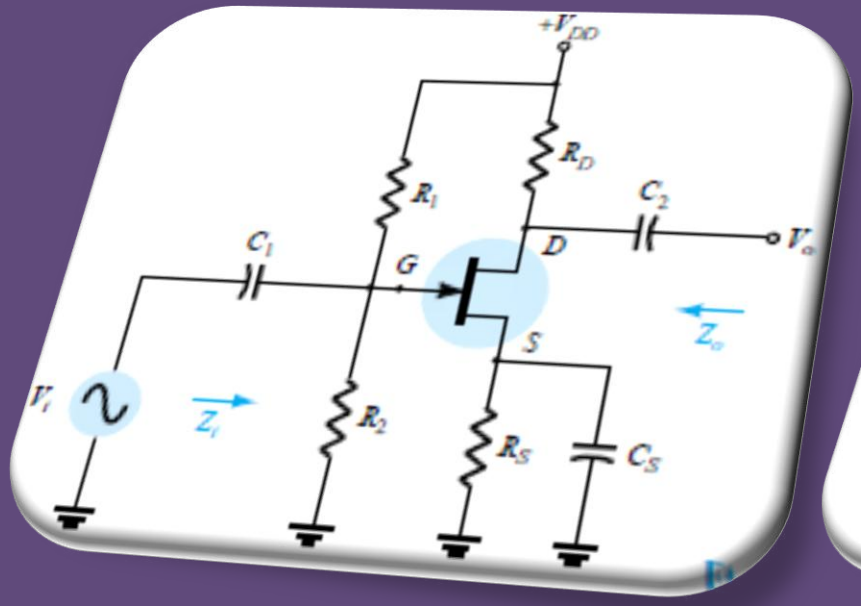
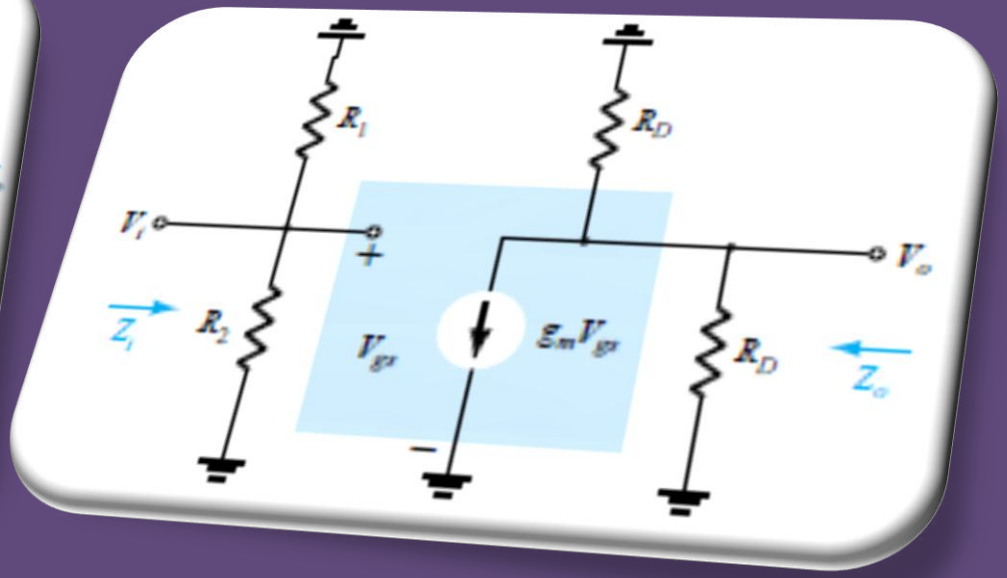
Electronic Circuits /2/

Dr. Nidal ZAIDAN

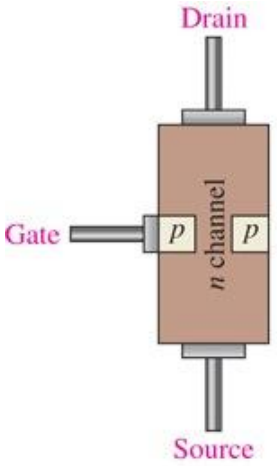
CHAPTER /2/

DESIGN OF FET AMPLIFIERS

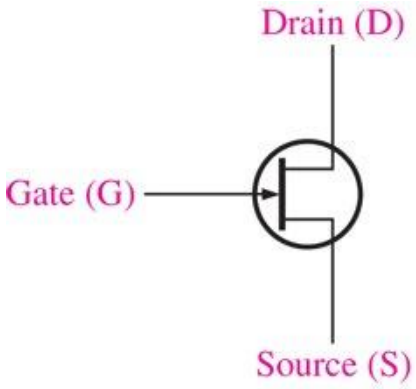




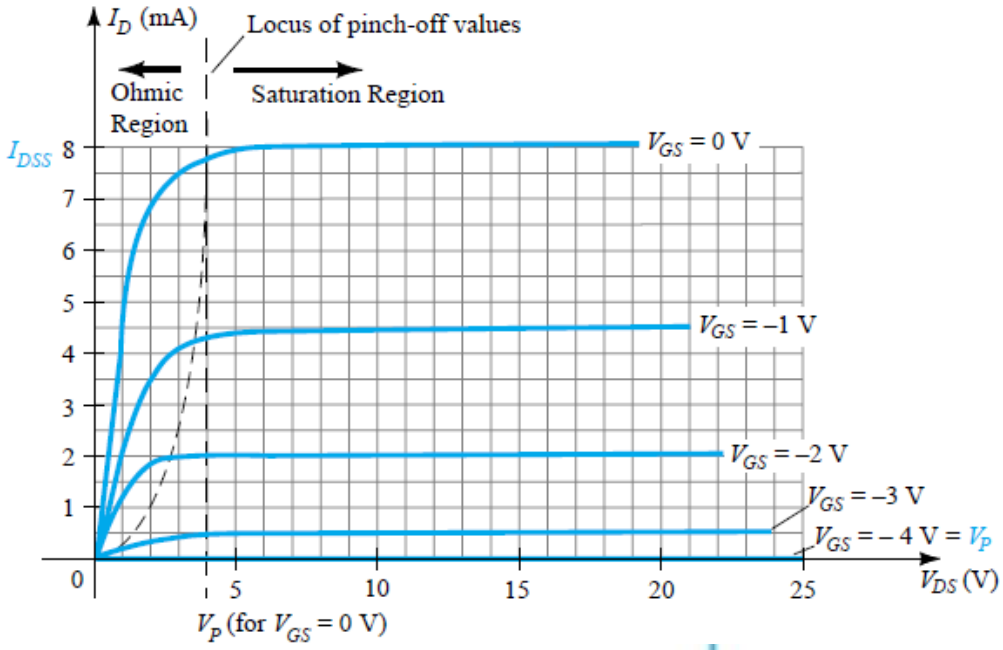
1. Basic Structure of The Two Type of JFET

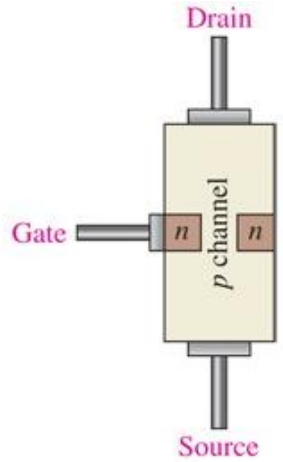


(a) *n* channel

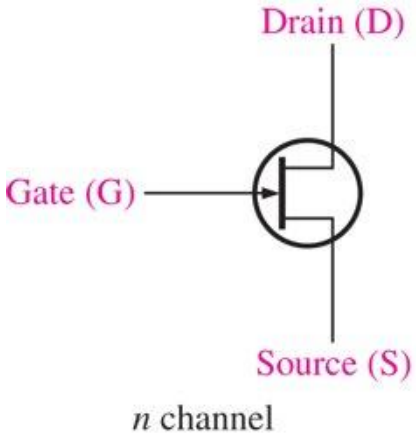


n channel

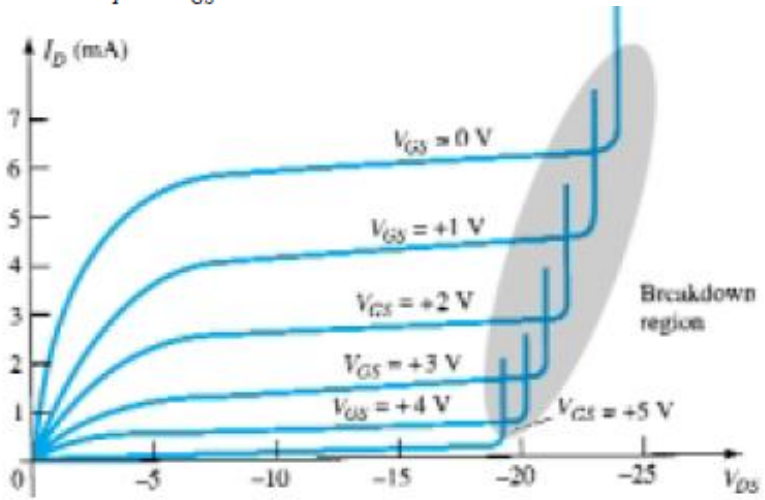




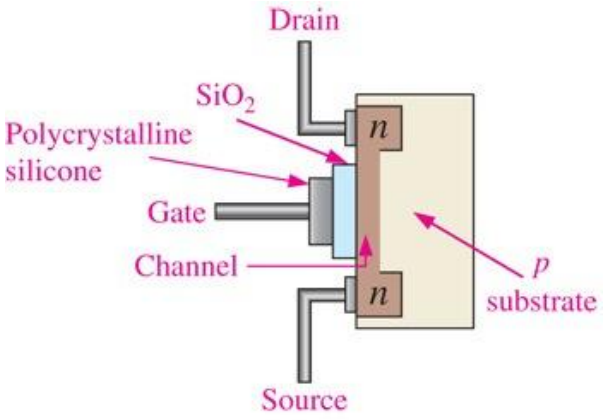
(b) *p* channel



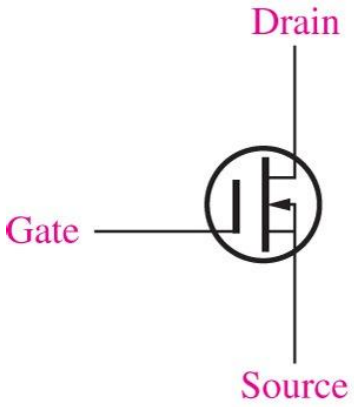
n channel



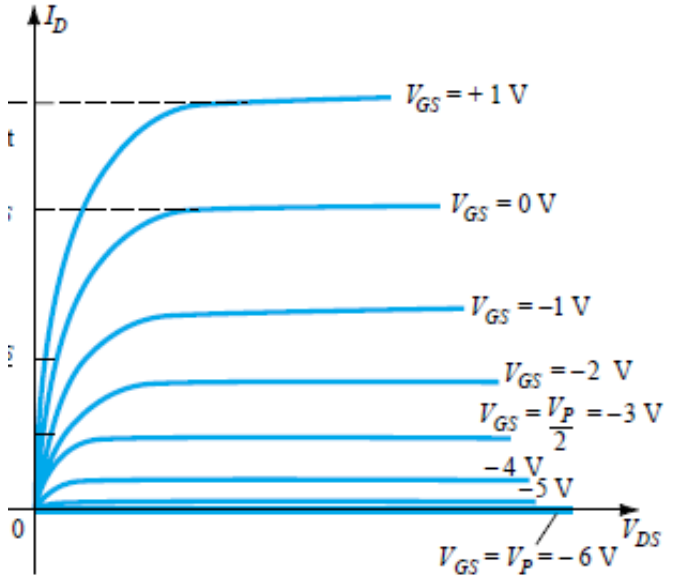
2. Basic Structure of D-MOSFETS

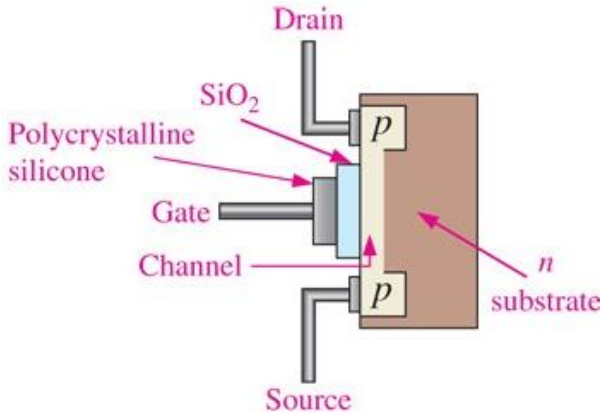


(a) *n* channel

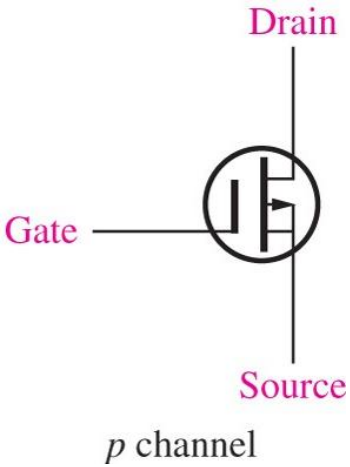


n channel

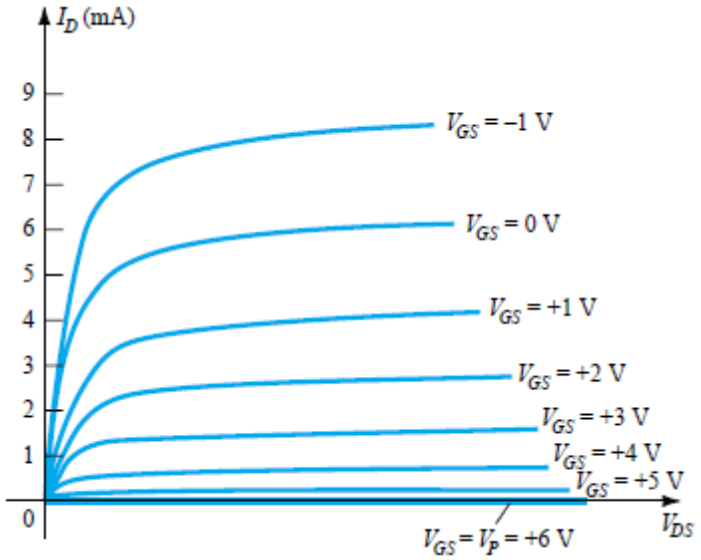




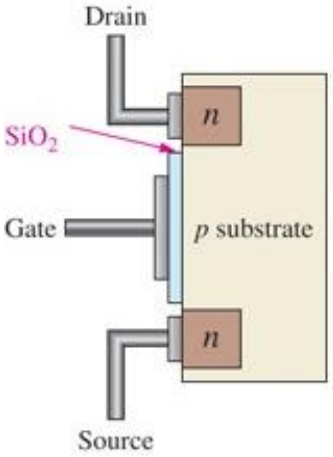
(b) *p* channel

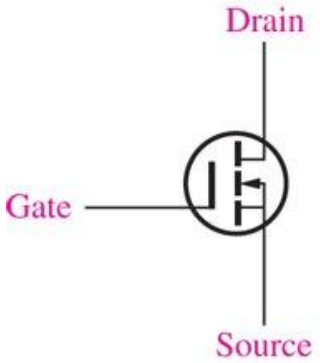


p channel

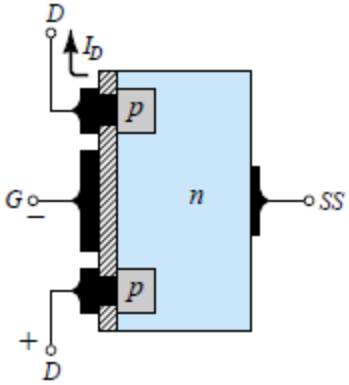


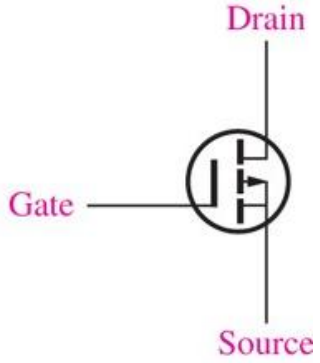
3. Basic Structure of E-MOSFETS



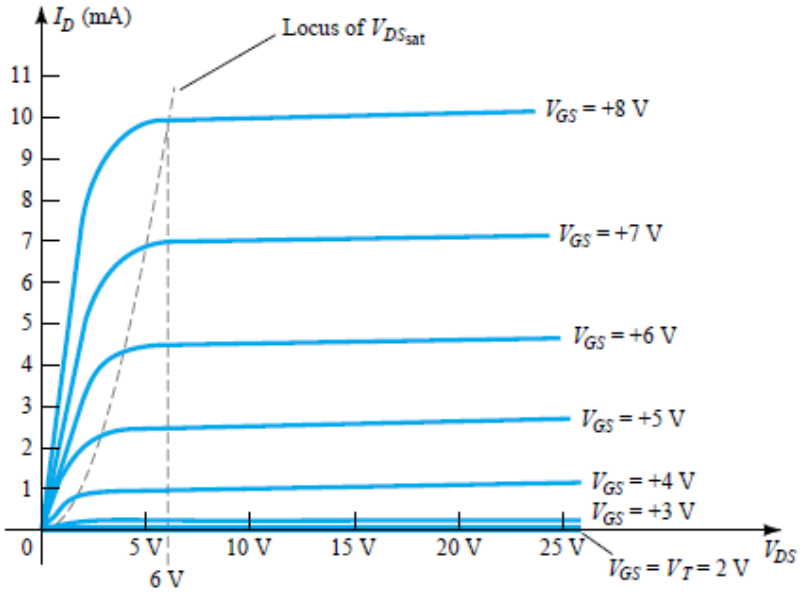


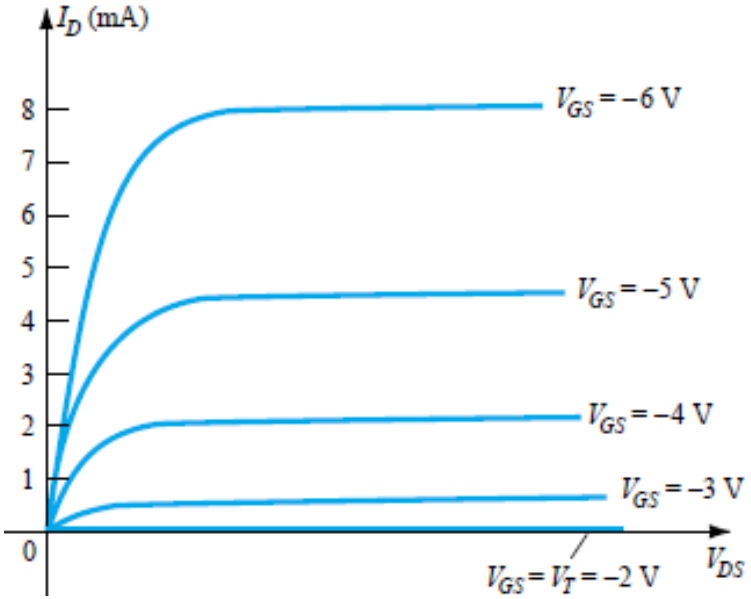
n channel





p channel





4. FET Biasing

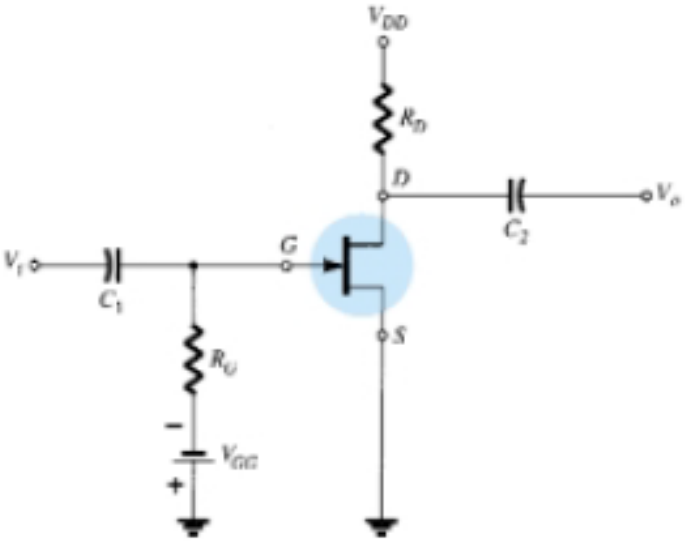
For JFETs and depletion-type MOSFETs, Shockley's equation is applied to relate the input and output quantities

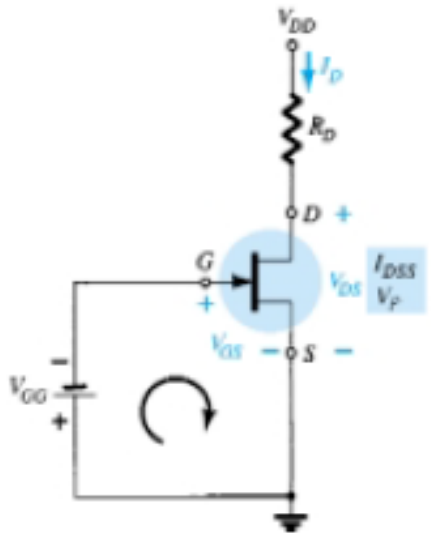
$$I_D = I_{DSS}(1 - \frac{V_{GS}}{V_P})^2$$

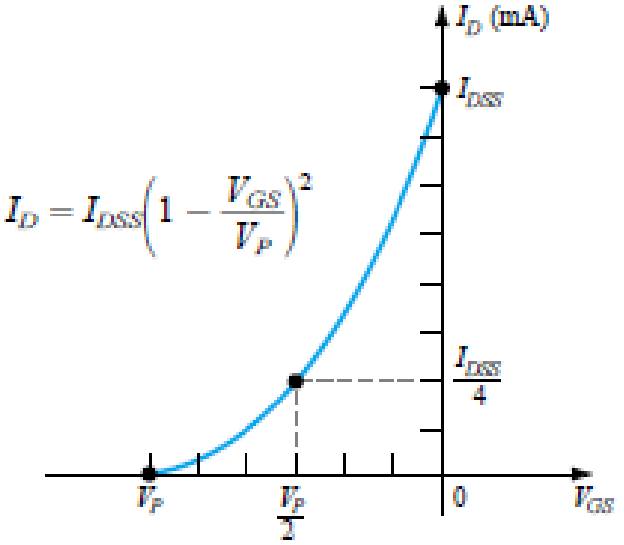
For enhancement-type MOSFETs, the following equation is applicable

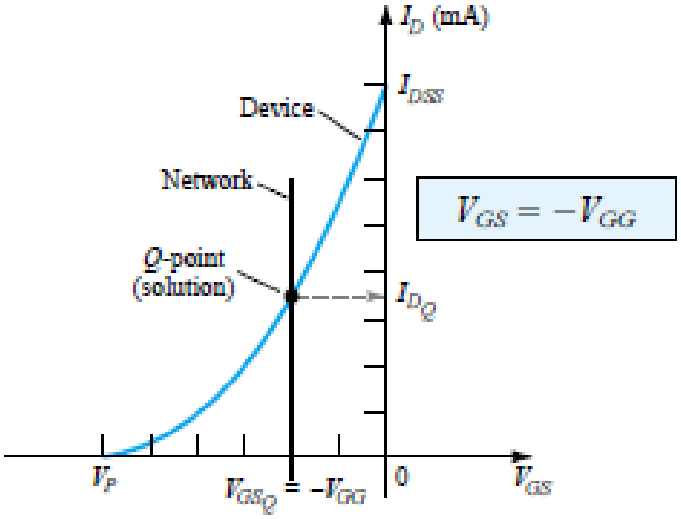
$$I_D = k(V_{GS} - V_T)^2$$

4.1. Fixed Bias Configuration





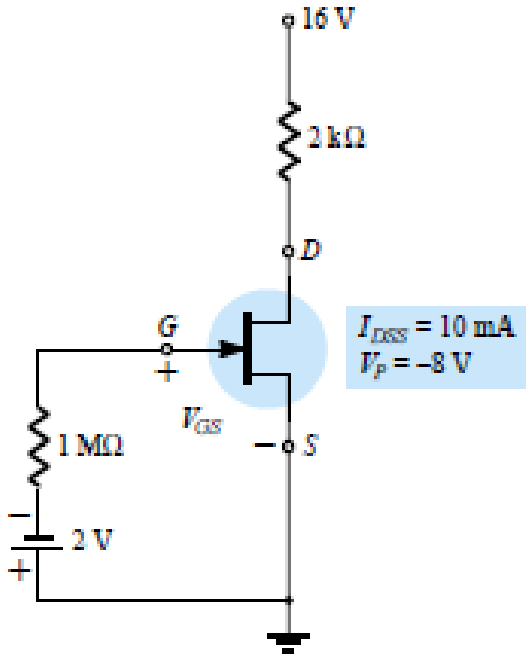




Example 1

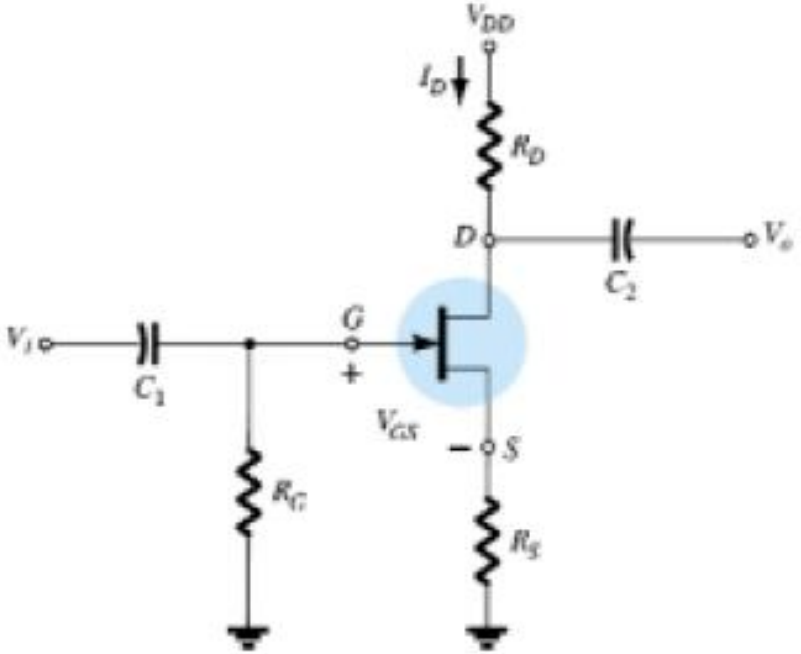
Determine the following for the network

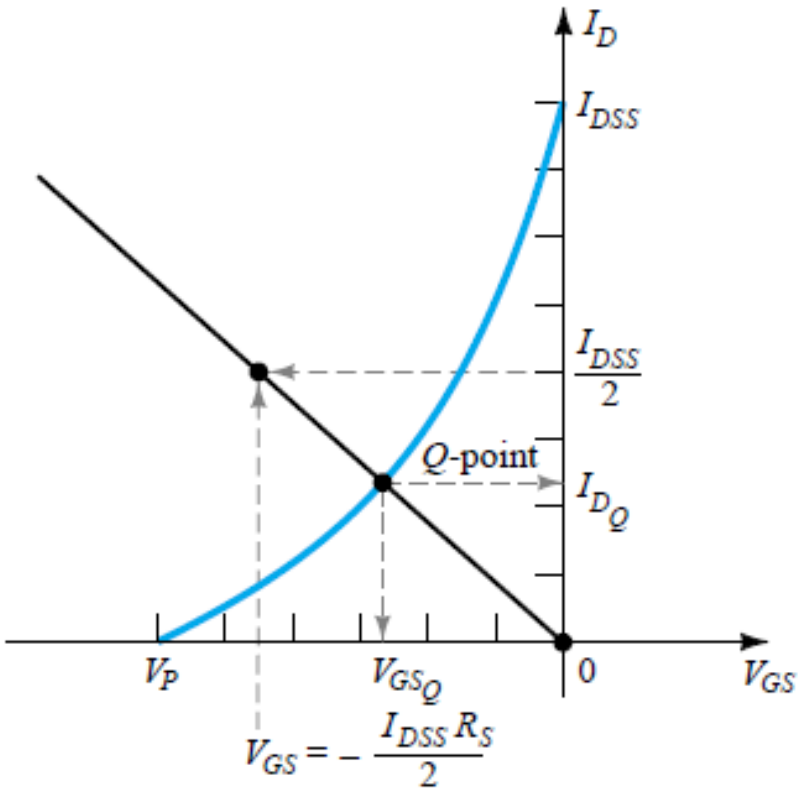
(a) V_{GS_Q}.
(b) I_{D_Q}.
(c) V_{DS}.
(d) V_D.
(e) V_G.
(f) V_S.



Solution

4.2. Self-Bias Configuration



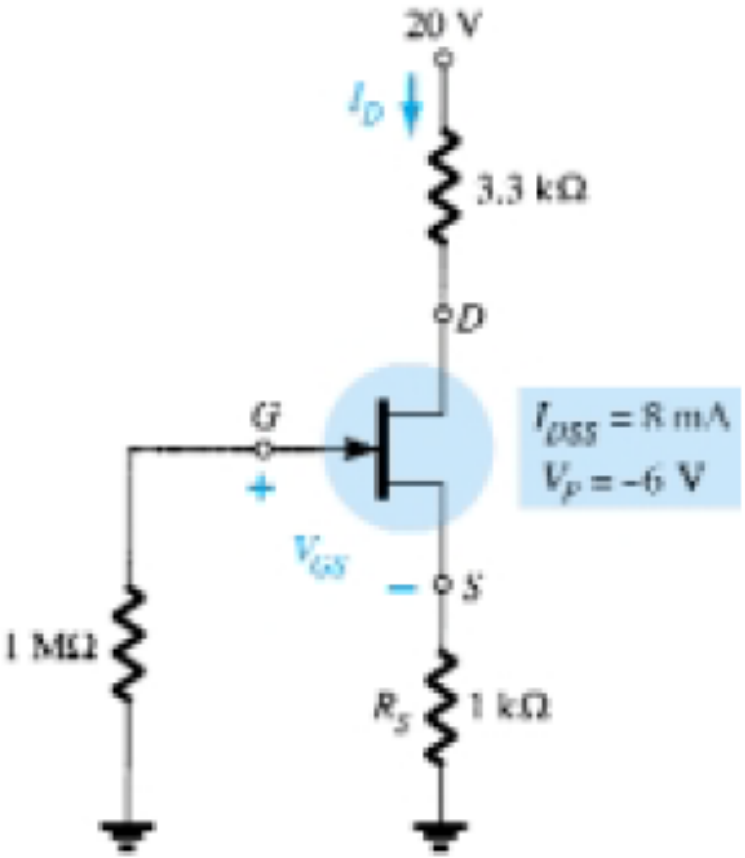


$$V_{GS} = -I_D R_S$$

Example 2

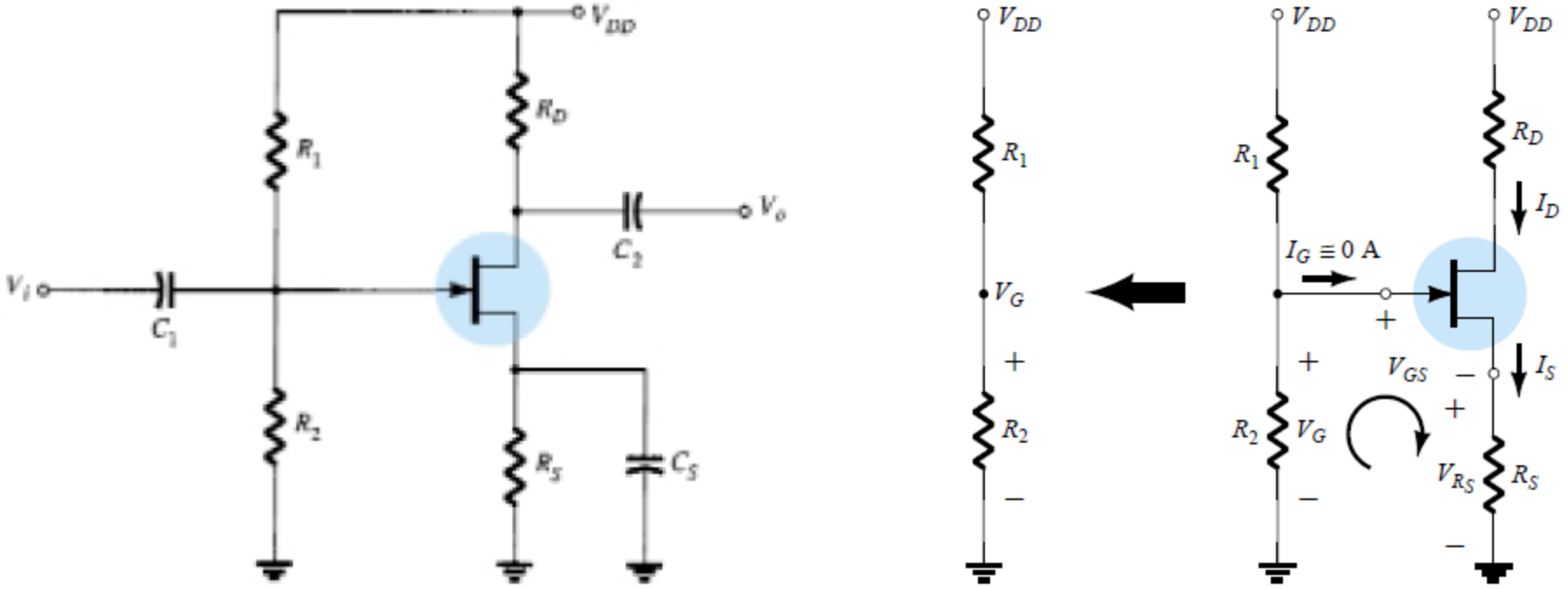
Determine the following for the network

(a) V_{GS_Q}.
(b) I_{D_Q}.
(c) V_{DS}.
(d) V_S.
(e) V_G.
(f) V_D.



Solution

4.3. Voltage-Divider Biasing

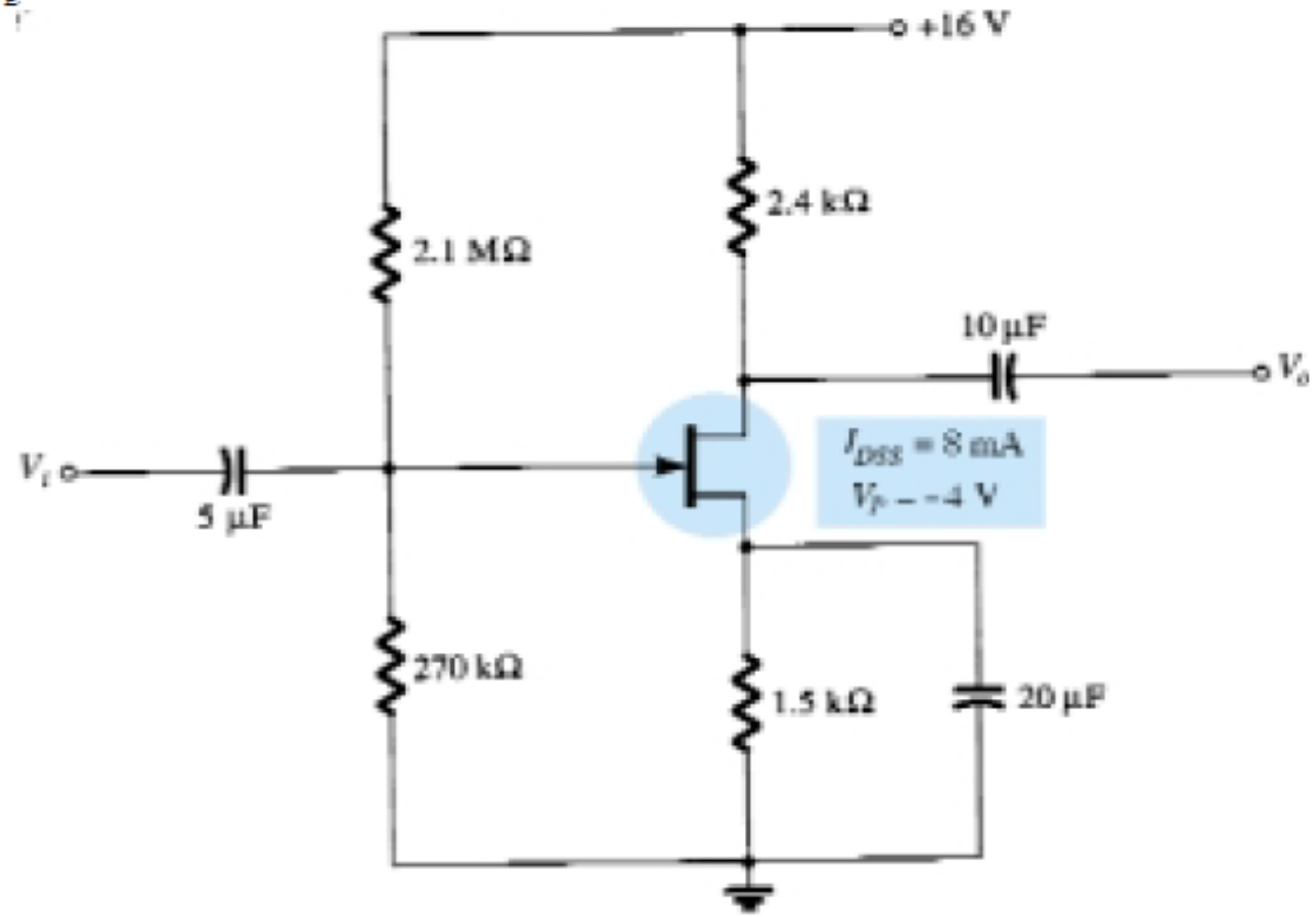


$$V_{GS} = V_G - I_D R_S$$

Example 3

Determine the following for the network

(a) I_{DQ} and V_{GSQ}.
(b) V_D.
(c) V_S.
(d) V_{DS}.
(e) V_{DG}.



Solution

5. FET Small Signal Model

The gate-to-source voltage controls the drain-to-source (channel) current of an FET

$$\Delta I_D = g_m \, \Delta V_{GS}$$

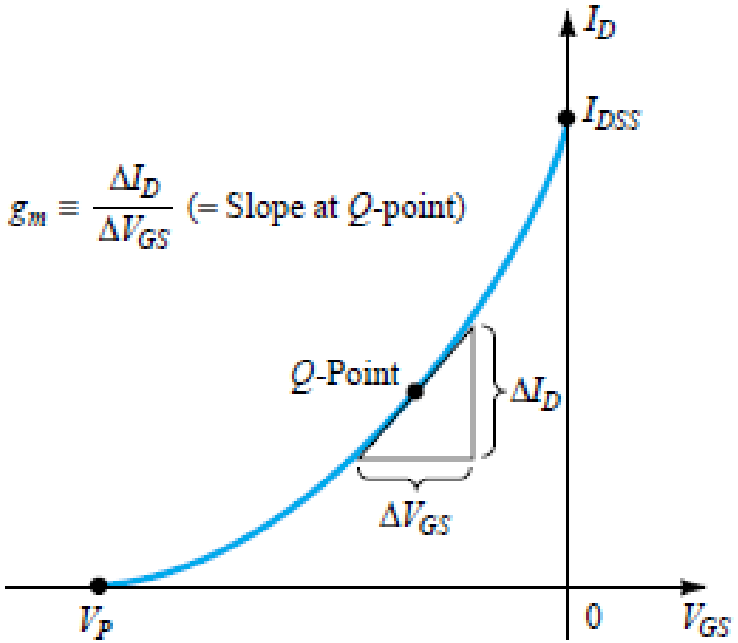
$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

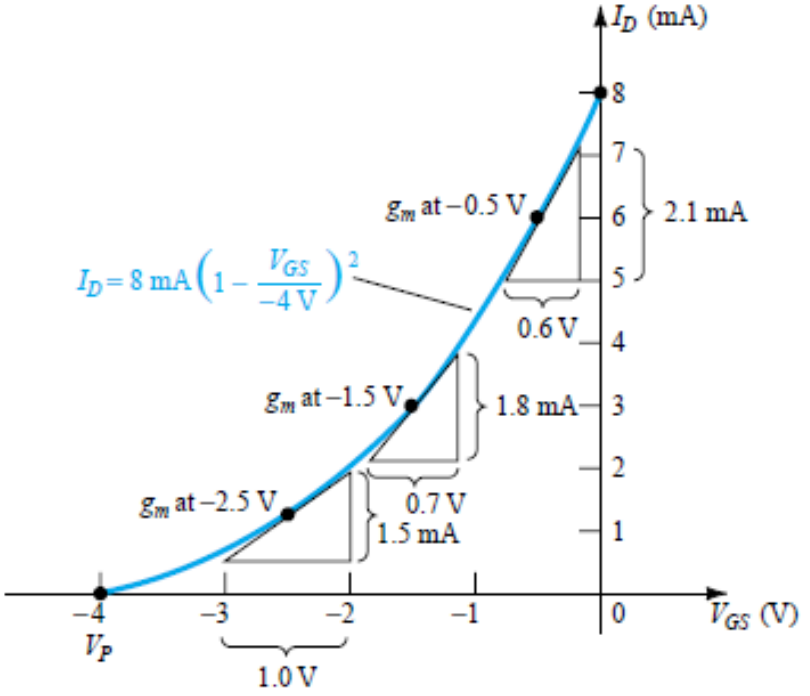
$$g_m = m = \frac{\Delta y}{\Delta x} = \frac{\Delta I_D}{\Delta V_{GS}}$$

(a) $g_m = \dfrac{\Delta I_D}{\Delta V_{GS}} \cong \dfrac{2.1 \text{ mA}}{0.6 \text{ V}} = \mathbf{3.5 \text{ mS}}$

(b) $g_m = \dfrac{\Delta I_D}{\Delta V_{GS}} \cong \dfrac{1.8 \text{ mA}}{0.7 \text{ V}} \cong \mathbf{2.57 \text{ mS}}$

(c) $g_m = \dfrac{\Delta I_D}{\Delta V_{GS}} = \dfrac{1.5 \text{ mA}}{1.0 \text{ V}} = \mathbf{1.5 \text{ mS}}$





Mathematical Definition of gm

If we therefore take the derivative of I_D with respect to V_{GS} (differential calculus) using Shockley's equation, an equation for g_m can be derived as follows:

$$g_m = \left.\frac{\Delta I_D}{\Delta V_{GS}}\right|_{Q\text{-pt.}} = \left.\frac{dI_D}{dV_{GS}}\right|_{Q\text{-pt.}} = \frac{d}{dV_{GS}}\left[I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2\right]$$

$$= I_{DSS}\frac{d}{dV_{GS}}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = 2I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]\frac{d}{dV_{GS}}\left(1 - \frac{V_{GS}}{V_P}\right)$$

$$= 2I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]\left[\frac{d}{dV_{GS}}(1) - \frac{1}{V_P}\frac{dV_{GS}}{dV_{GS}}\right] = 2I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]\left[0 - \frac{1}{V_P}\right]$$

and

$$g_m = \frac{2I_{DSS}}{|V_P|}\left[1 - \frac{V_{GS}}{V_P}\right]$$

$V_{GS} = 0$ V. ⟹

$$g_m = \frac{2I_{DSS}}{|V_P|}\left[1 - \frac{0}{V_P}\right]$$

$$g_{m0} = \frac{2I_{DSS}}{|V_P|}$$

$$g_m = g_{m0}\left(1 - \frac{V_{GS}}{V_P}\right) = g_{m0}\sqrt{\frac{I_D}{I_{DSS}}}$$

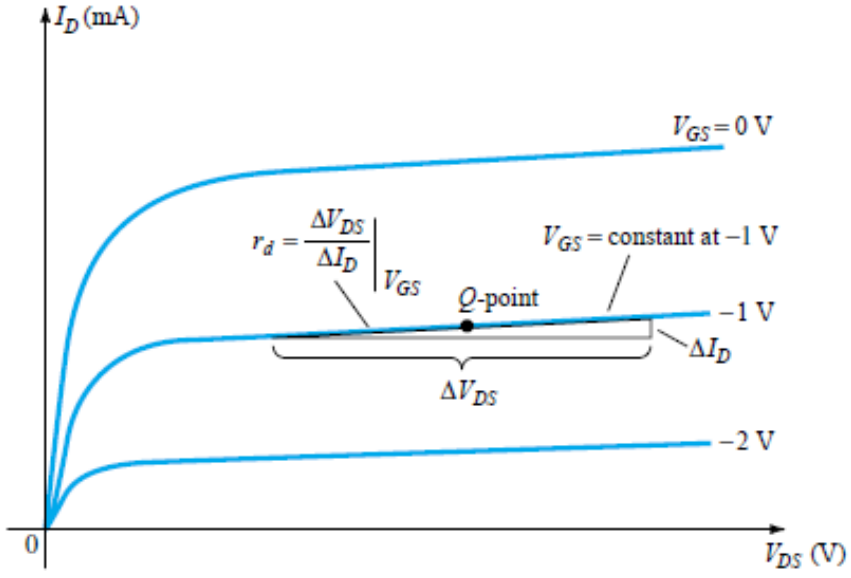
FET Input Impedance Zi

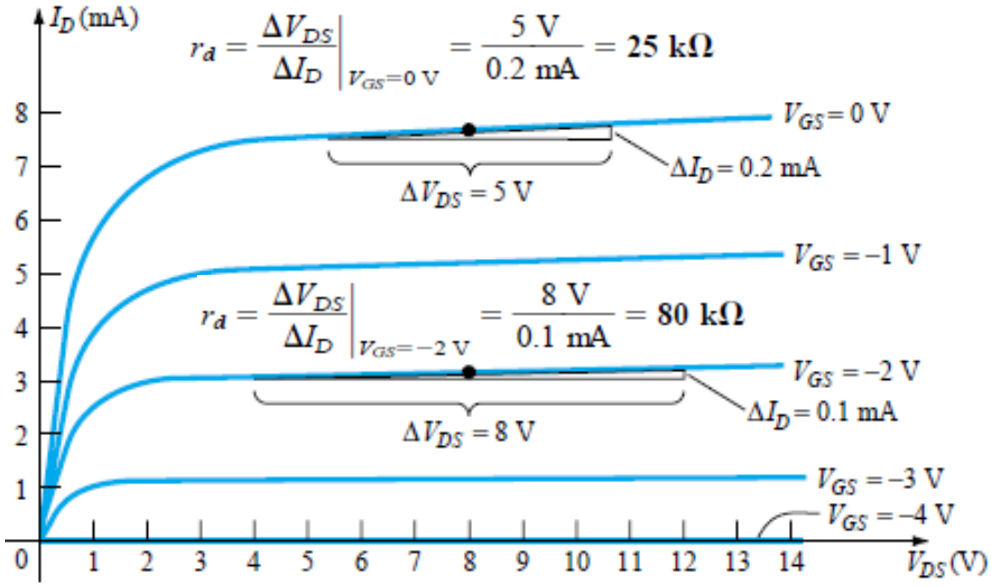
$$Z_i\ (\text{FET}) = \infty\ \Omega$$

FET Output Impedance Zo

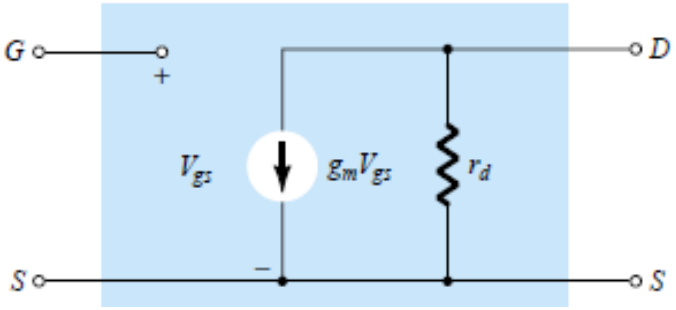
$$Z_o\ (\text{FET}) = r_d = \frac{1}{y_{os}}$$

$$r_d = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS}=\text{constant}}$$





FET AC Equivalent Ciruit

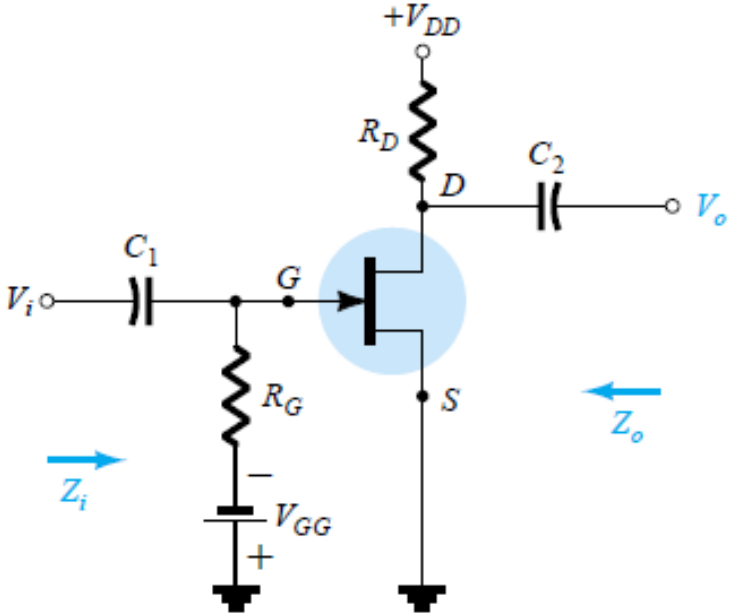


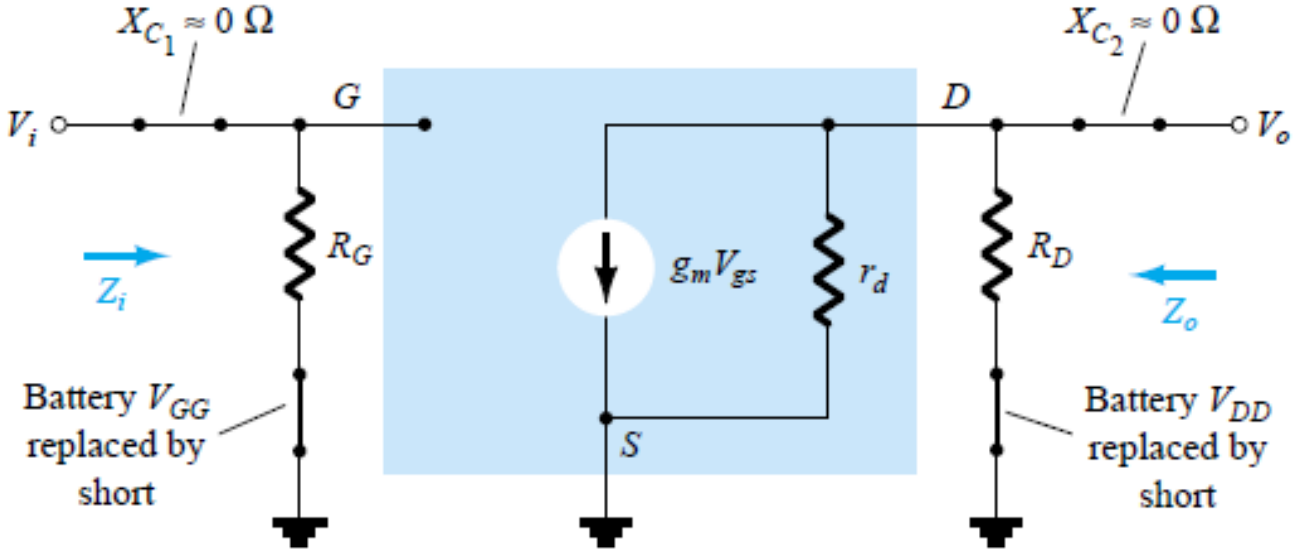
EXAMPLE

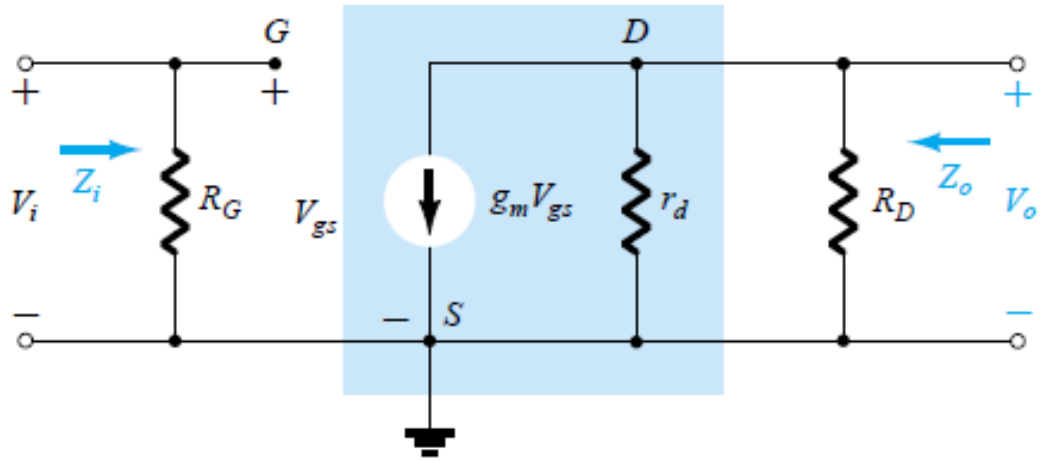
Given $y_{fs} = 3.8$ mS and $y_{os} = 20\ \mu$S, sketch the FET ac equivalent model.

Solution

5.1. JFET Fixed Bias Configuration

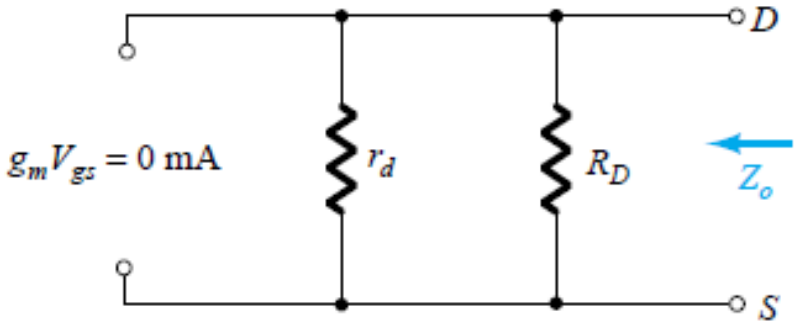






$$Z_i = R_G$$

Z_o: Setting $V_i = 0$ V as required by the definition of Z_o will establish V_{gs} as 0 V also. The result is $g_m V_{gs} = 0$ mA, and the current source can be replaced by an open-circuit equivalent as shown in Fig. 9.13. The output impedance is



$$Z_o = R_D \| r_d$$

$$V_o = -g_m V_{gs}(r_d \| R_D)$$

but $V_{gs} = V_i$

and $$V_o = -g_m V_i(r_d \| R_D)$$

so that

$$\boxed{A_v = \frac{V_o}{V_i} = -g_m(r_d \| R_D)}$$

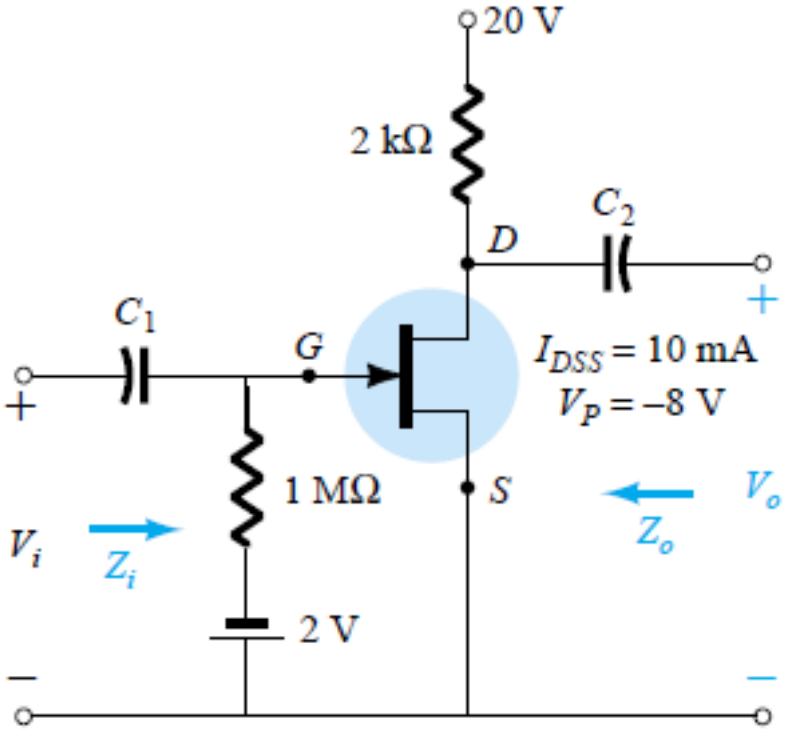
If $r_d \geq 10R_D$:

$$\boxed{A_v = \frac{V_o}{V_i} = -g_m R_D}_{r_d \geq 10R_D}$$

Example 4

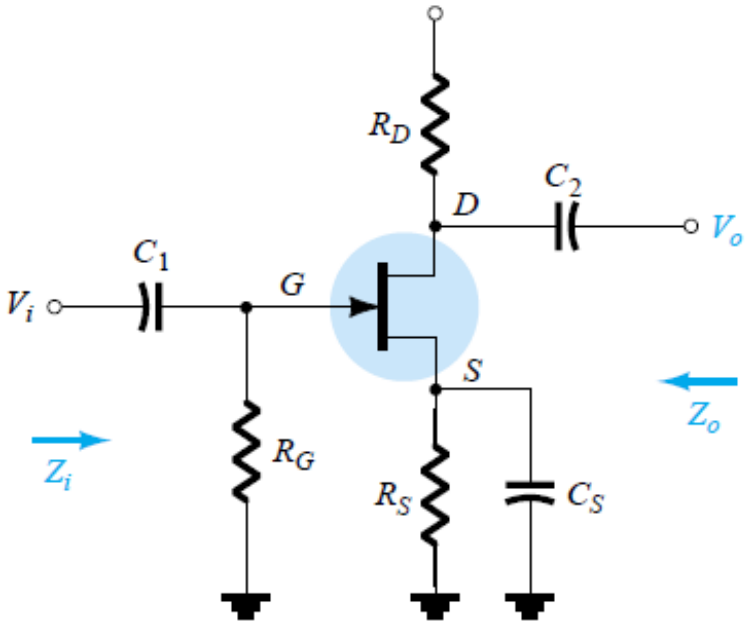
The fixed-bias configuration of Example 1 had an operating point defined by $V_{GS_Q} = -2$ V and $I_{D_Q} = 5.625$ mA, with $I_{DSS} = 10$ mA and $V_P = -8$ V. The network is redrawn as Fig. 9.14 with an applied signal V_i. The value of y_{os} is provided as 40 μS.

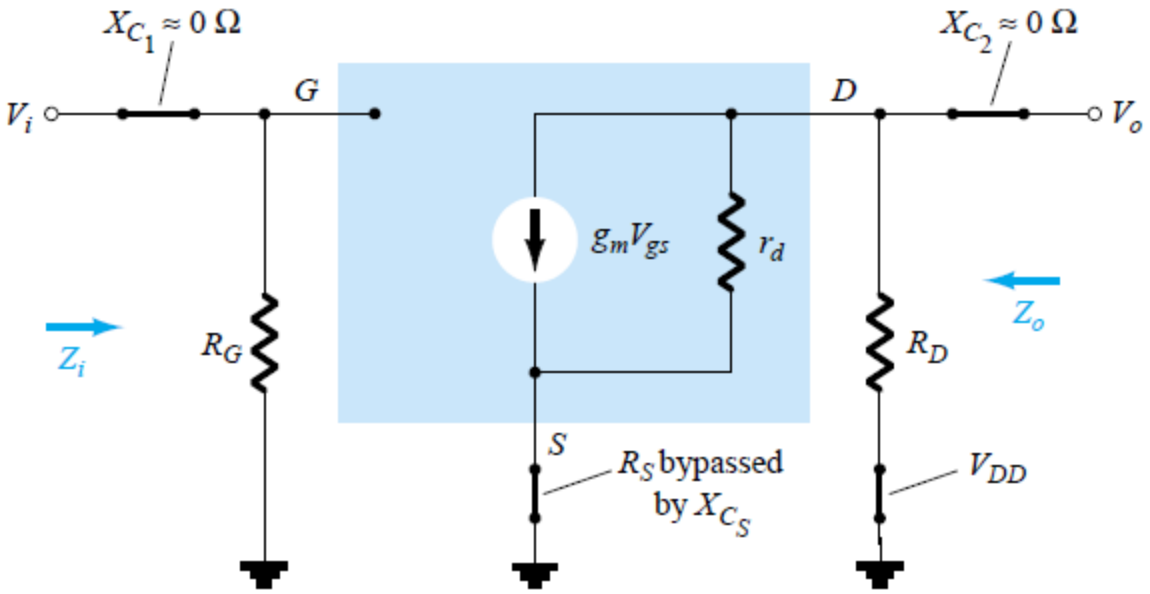
(a) Determine g_m.
(b) Find r_d.
(c) Determine Z_i.
(d) Calculate Z_o.
(e) Determine the voltage gain A_v.
(f) Determine A_v ignoring the effects of r_d.

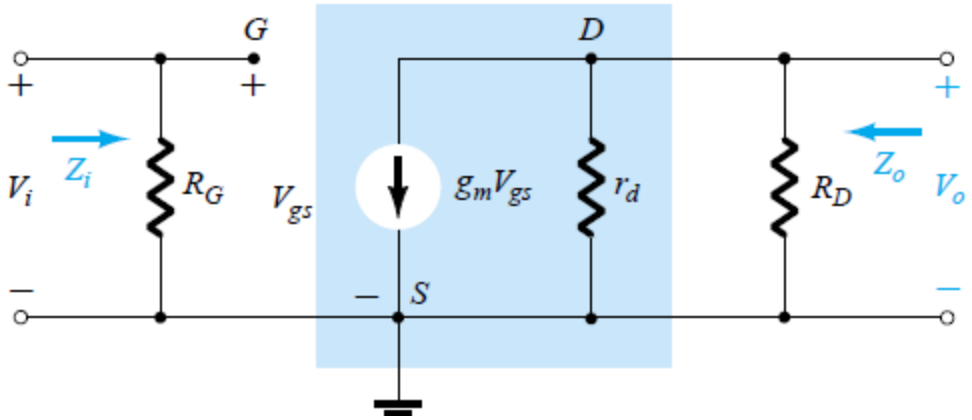


Solution

5.2. JFET Self-Bias Configuration







Z_i:

$$Z_i = R_G$$

Z_o:

$$Z_o = r_d \| R_D$$

If $r_d \geq 10R_D$,

$$Z_o \cong R_D \quad r_d \geq 10R_D$$

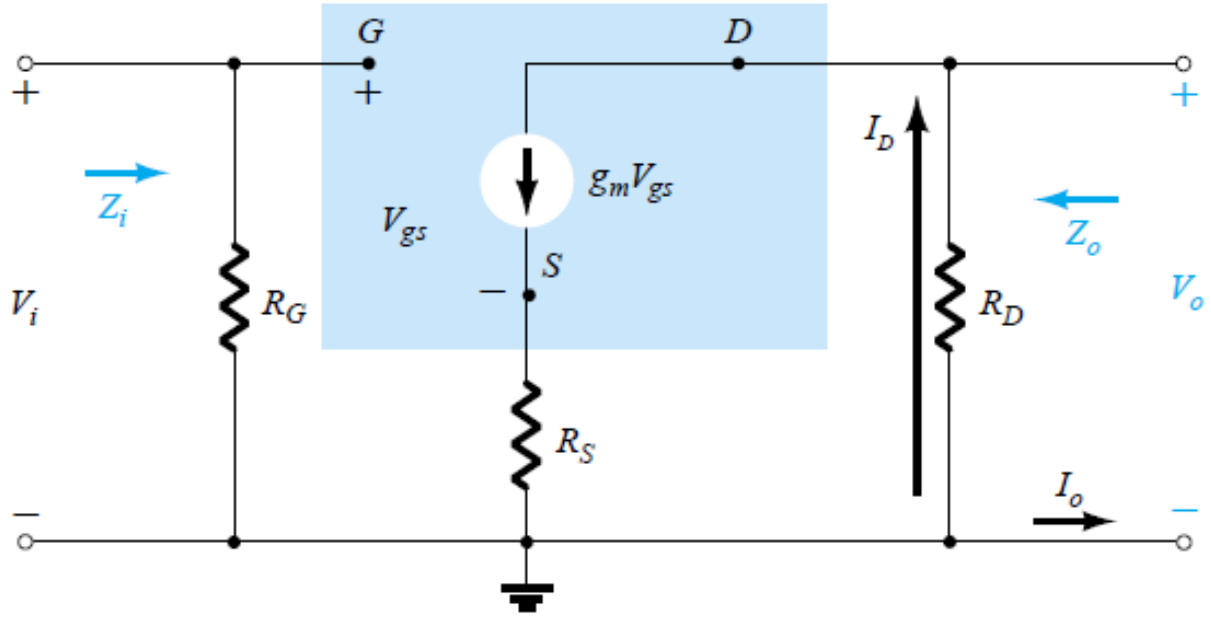
A_v:

$$A_v = -g_m(r_d \| R_D)$$

If $r_d \geq 10R_D$,

$$A_v = -g_m R_D \quad r_d \geq 10R_D$$

Unbypassed Rs



Z_i: Due to the open-circuit condition between the gate and output network, the input remains the following:

$$Z_i = R_G \tag{9.23}$$

Z_o: The output impedance is defined by

$$Z_o = \left.\frac{V_o}{I_o}\right|_{V_i = 0}$$

Applying Kirchhoff's current law will result in:

$$I_o + I_D = g_m V_{gs}$$

with $$V_{gs} = -(I_o + I_D)R_S$$

so that $$I_o + I_D = -g_m (I_o + I_D)R_S = -g_m I_o R_S - g_m I_D R_S$$

or $$I_o[1 + g_m R_S] = -I_D[1 + g_m R_S]$$

and $I_o = -I_D$ (the controlled current source $g_m V_{gs} = 0$ A for the applied conditions)

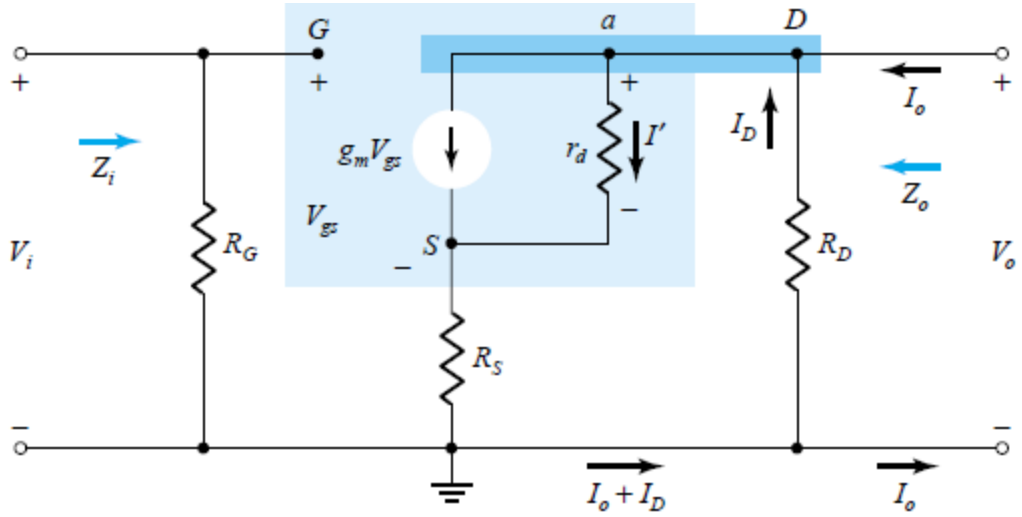
Since $$V_o = -I_D R_D$$

then $$V_o = -(-I_o)R_D = I_o R_D$$

and $$\boxed{Z_o = \frac{V_o}{I_o} = R_D}$$

$r_d = \infty\Omega$

If r_d is included in the network



Since
$$Z_o = \left.\frac{V_o}{I_o}\right|_{V_i = 0\text{ V}} = -\frac{I_D R_D}{I_o}$$

we should try to find an expression for I_o in terms of I_D.

Applying Kirchhoff's current law:

$$I_o = g_m V_{gs} + I_{r_d} - I_D$$

but
$$V_{r_d} = V_o + V_{gs}$$

and
$$I_o = g_m V_{gs} + \frac{V_o + V_{gs}}{r_d} - I_D$$

or
$$I_o = \left(g_m + \frac{1}{r_d}\right) V_{gs} - \frac{I_D R_D}{r_d} - I_D \text{ using } V_o = -I_D R_D$$

Now, $$V_{gs} = -(I_D + I_o)\, R_S$$

so that $$I_o = -\left(g_m + \frac{1}{r_d}\right)(I_D + I_o)\, R_S - \frac{I_D R_D}{r_d} - I_D$$

with the result that $$I_o\left[1 + g_m R_s + \frac{R_S}{r_d}\right] = -I_D\left[1 + g_m R_S + \frac{R_S}{r_d} + \frac{R_D}{r_d}\right]$$

or $$I_o = \frac{-I_D\left[1 + g_m R_S + \frac{R_S}{r_d} + \frac{R_D}{r_d}\right]}{1 + g_m R_S + \frac{R_S}{r_d}}$$

and $$Z_o = \frac{V_o}{I_o} = \frac{-I_D R_D}{\dfrac{-I_D\left(1 + g_m R_s + \frac{R_s}{r_d} + \frac{R_D}{r_d}\right)}{1 + g_m R_S + \frac{R_S}{r_d}}}$$

and finally, $$\boxed{Z_o = \frac{\left[1 + g_m R_S + \frac{R_S}{r_d}\right]}{\left[1 + g_m R_S + \frac{R_S}{r_d} + \frac{R_D}{r_d}\right]} R_D}$$

For $r_d \geq 10\,R_D$, $\left(1 + g_m R_S + \dfrac{R_S}{r_d}\right) >> \dfrac{R_D}{r_d}$ and $1 + g_m R_S + \dfrac{R_S}{r_d} + \dfrac{R_D}{r_d}$

$\cong 1 + g_m R_S + \dfrac{R_S}{r_d}$ and

$$\boxed{Z_o = R_D}_{r_d \geq 10R_D}$$

A_v: For the network of Fig. 9.19, an application of Kirchhoff's voltage law on the input circuit will result in

$$V_i - V_{gs} - V_{R_S} = 0$$

$$V_{gs} = V_i - I_D R_S$$

The voltage across r_d using Kirchhoff's voltage law is

$$V_o - V_{R_S}$$

and

$$I' = \frac{V_o - V_{R_S}}{r_d}$$

so that an application of Kirchhoff's current law will result in

$$I_D = g_m V_{gs} + \frac{V_o - V_{R_S}}{r_d}$$

Substituting for V_{gs} from above and substituting for V_o and V_{R_S} we have

$$I_D = g_m[V_i - I_D R_S] + \frac{(-I_D R_D) - (I_D R_S)}{r_d}$$

so that

$$I_D\left[1 + g_m R_S + \frac{R_D + R_S}{r_d}\right] = g_m V_i$$

or

$$I_D = \frac{g_m V_i}{1 + g_m R_S + \frac{R_D + R_S}{r_d}}$$

The output voltage is then

$$V_o = -I_D R_D = -\frac{g_m R_D V_i}{1 + g_m R_S + \frac{R_D + R_S}{r_d}}$$

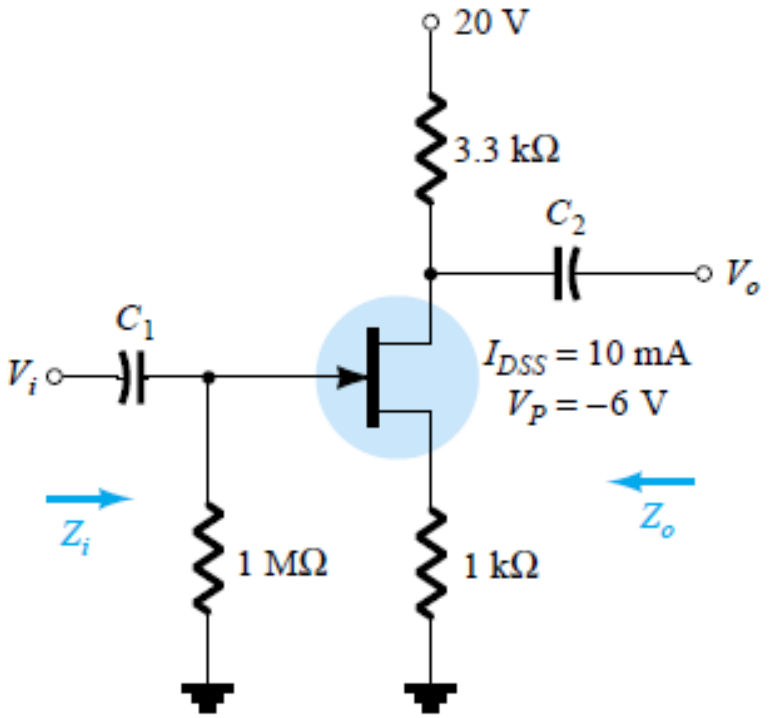
and

$$\boxed{A_v = \frac{V_o}{V_i} = -\frac{g_m R_D}{1 + g_m R_S + \frac{R_D + R_S}{r_d}}}$$

Example 5

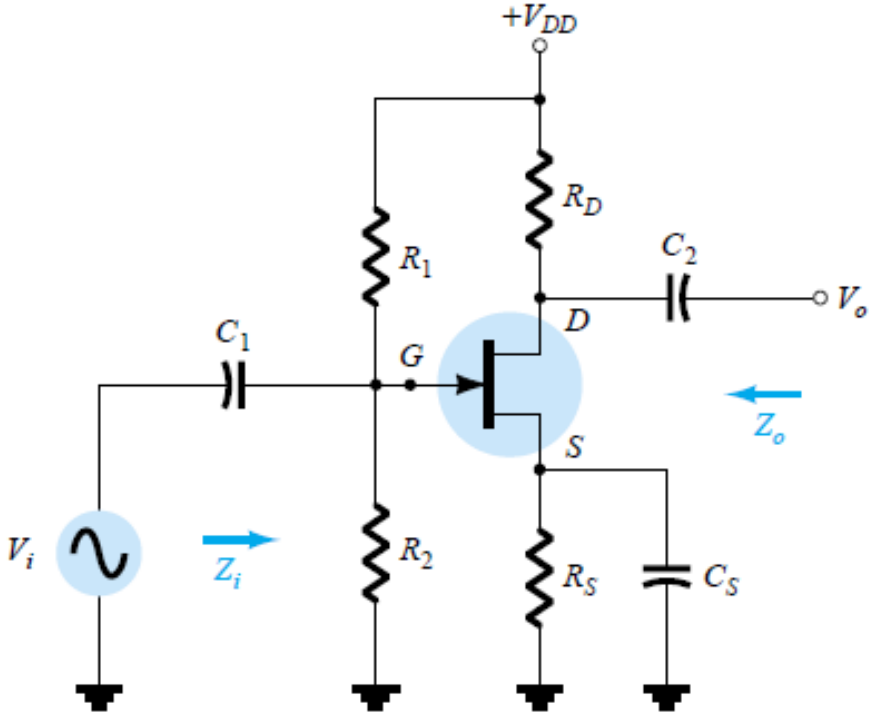
The self-bias configuration of Example 2 has an operating point defined by $V_{GS_Q} = -2.6$ V and $I_{D_Q} = 2.6$ mA, with $I_{DSS} = 8$ mA and $V_P = -6$ V. The network is redrawn as Fig. 9.20 with an applied signal V_i. The value of y_{os} is given as 20 μS.

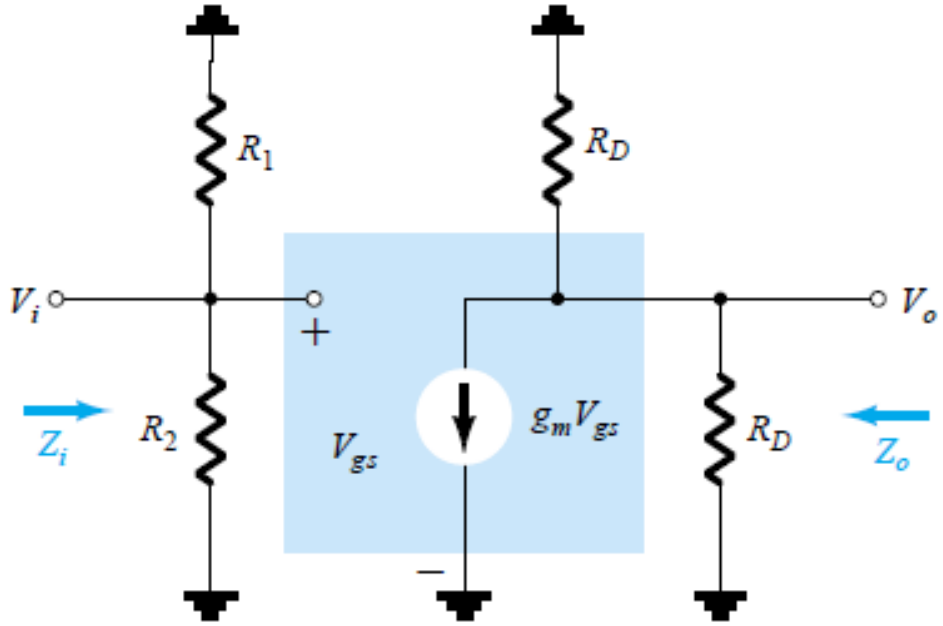
(a) Determine g_m.
(b) Find r_d.
(c) Find Z_i.
(d) Calculate Z_o with and without the effects of r_d. Compare the results.
(e) Calculate A_v with and without the effects of r_d. Compare the results.

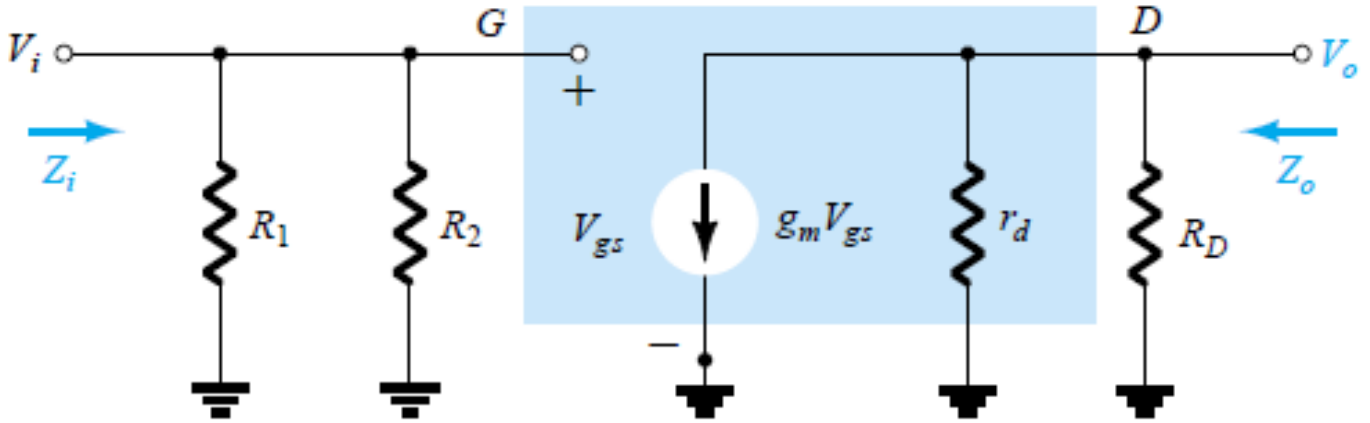


Solution

5.3. JFET Voltage-Divider Configuration







Z_i: R_1 and R_2 are in parallel with the open-circuit equivalence of the JFET resulting in

$$Z_i = R_1 \| R_2$$

Z_o: Setting $V_i = 0$ V will set V_{gs} and $g_m V_{gs}$ to zero and

$$Z_o = r_d \| R_D$$

For $r_d \geq 10R_D$,

$$Z_o \cong R_D \qquad r_d \geq 10R_D$$

A_v:

$$V_{gs} = V_i$$

and

$$V_o = -g_m V_{gs}(r_d \| R_D)$$

so that

$$A_v = \frac{V_o}{V_i} = \frac{-g_m V_{gs}(r_d \| R_D)}{V_{gs}}$$

and

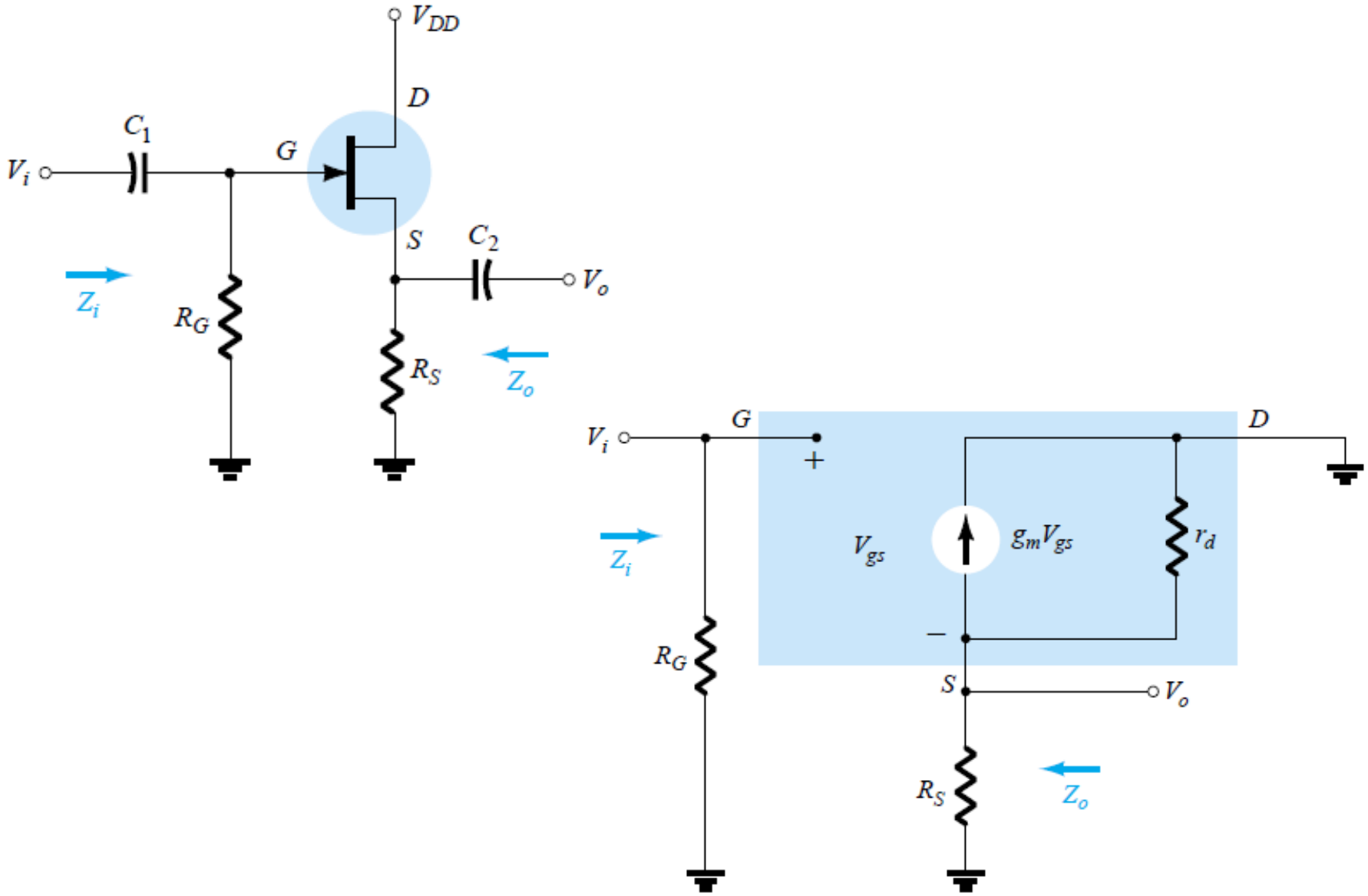
$$\boxed{A_v = \frac{V_o}{V_i} = -g_m(r_d \| R_D)}$$

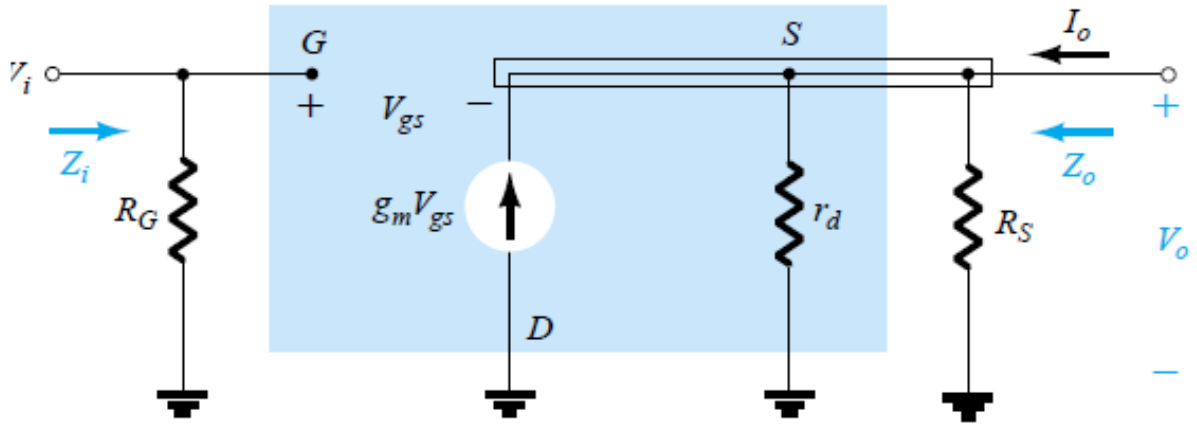
If $r_d \geq 10R_D$,

$$\boxed{A_v = \frac{V_o}{V_i} \cong -g_m R_D} \quad r_d \geq 10R_D$$

Note that the equations for Z_o and A_v are the same as obtained for the fixed-bias and self-bias (with bypassed R_S) configurations. The only difference is the equation for Z_i, which is now sensitive to the parallel combination of R_1 and R_2.

5.4. JFET Source Follower (Common-Drain) Configuration

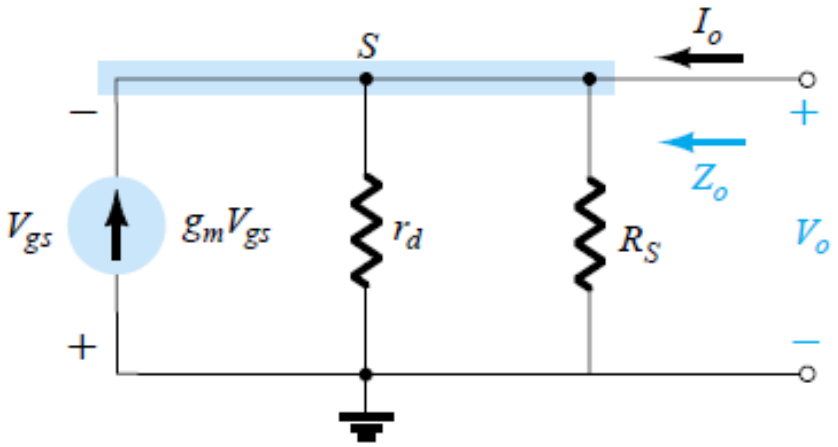




$$Z_i = R_G$$

$\boldsymbol{Z_o}$: Setting $V_i = 0$ V will result in the gate terminal being connected directly to ground

The fact that V_{gs} and V_o are across the same parallel network results in $V_o = -V_{gs}$.



Applying Kirchhoff's current law at node s,

$$I_o + g_m V_{gs} = I_{r_d} + I_{R_S}$$

$$= \frac{V_o}{r_d} + \frac{V_o}{R_S}$$

The result is

$$I_o = V_o\left[\frac{1}{r_d} + \frac{1}{R_S}\right] - g_m V_{gs}$$

$$= V_o\left[\frac{1}{r_d} + \frac{1}{R_S}\right] - g_m[-V_o]$$

$$= V_o\left[\frac{1}{r_d} + \frac{1}{R_S} + g_m\right]$$

and $$Z_o = \frac{V_o}{I_o} = \frac{V_o}{V_o\left[\frac{1}{r_d} + \frac{1}{R_S} + g_m\right]} = \frac{1}{\frac{1}{r_d} + \frac{1}{R_S} + g_m} = \frac{1}{\frac{1}{r_d} + \frac{1}{R_S} + \frac{1}{1/g_m}}$$

which has the same format as the total resistance of three parallel resistors. Therefore,

$$\boxed{Z_o = r_d \| R_S \| 1/g_m}$$

A_v: The output voltage V_o is determined by

$$V_o = g_m V_{gs}(r_d \| R_S)$$

and applying Kirchhoff's voltage law around the perimeter of the network will result in

$$V_i = V_{gs} + V_o$$

and

$$V_{gs} = V_i - V_o$$

so that

$$V_o = g_m(V_i - V_o)(r_d \| R_S)$$

or

$$V_o = g_m V_i(r_d \| R_S) - g_m V_o(r_d \| R_S)$$

and

$$V_o[1 + g_m(r_d \| R_S)] = g_m V_i(r_d \| R_S)$$

so that

$$\boxed{A_v = \frac{V_o}{V_i} = \frac{g_m(r_d \| R_S)}{1 + g_m(r_d \| R_S)}}$$

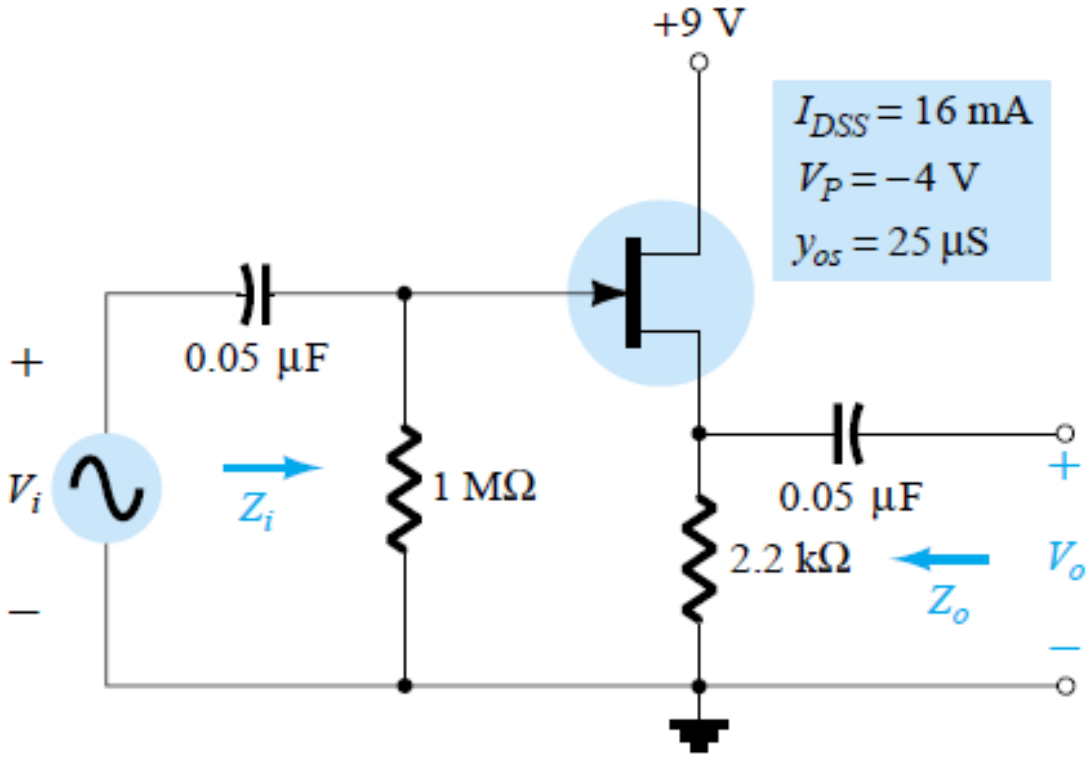
In the absence of r_d or if $r_d \geq 10R_S$,

$$\boxed{A_v = \frac{V_o}{V_i} \cong \frac{g_m R_S}{1 + g_m R_S}} \quad r_d \geq 10R_S$$

Example 6

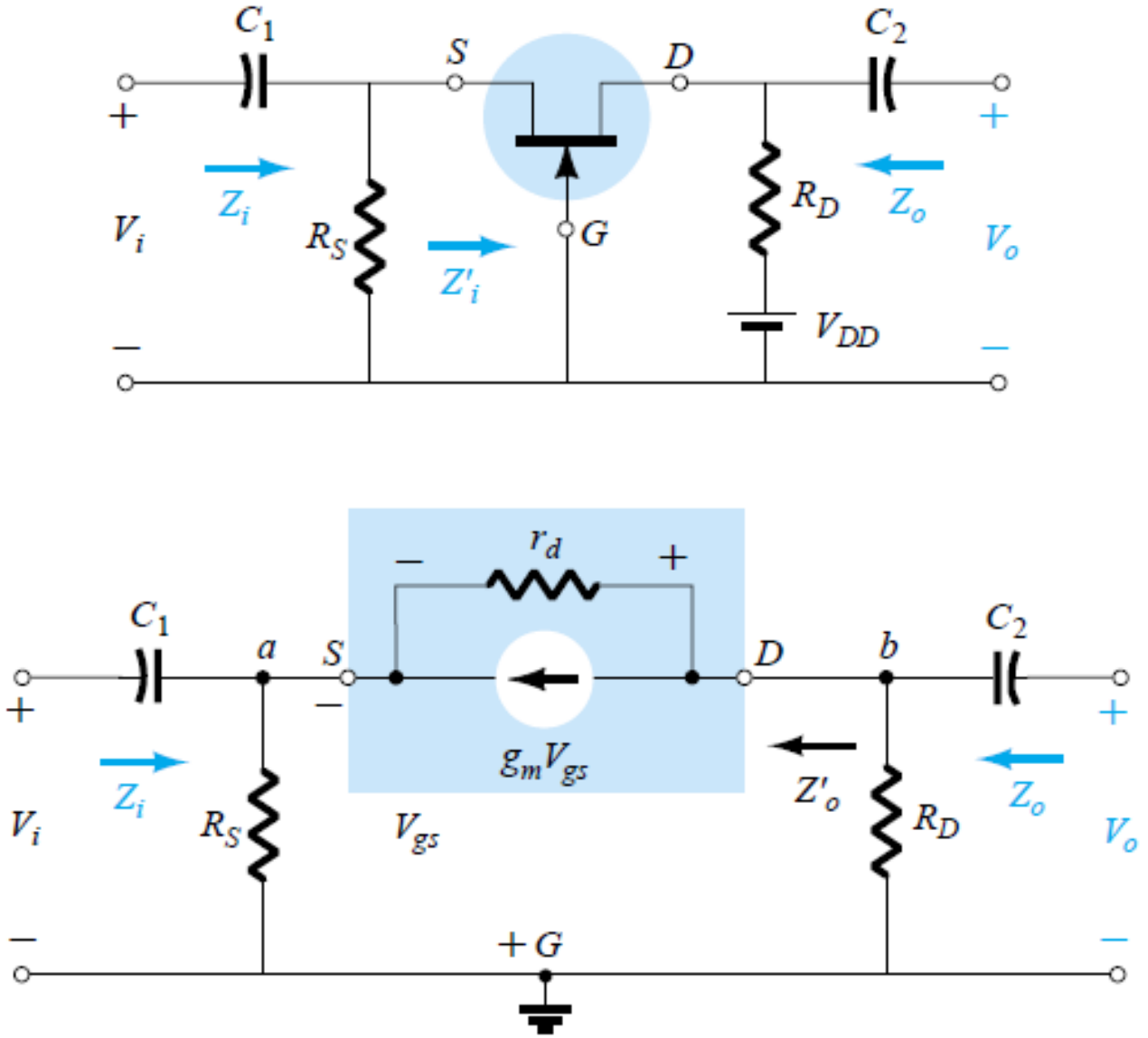
A dc analysis of the source-follower network will result in $V_{GS_Q} = -2.86$ V and $I_{D_Q} = 4.56$ mA.

(a) Determining g_m.
(b) Find r_d.
(c) Determine Z_i.
(d) Calculate Z_o with and without r_d. Compare results.
(e) Determine A_v with and without r_d. Compare results.

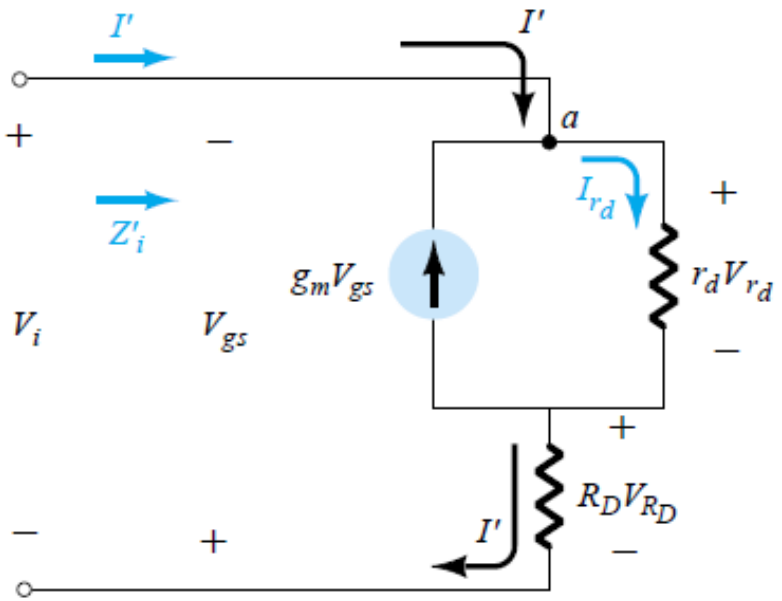


Solution

5.5. JFET Common-Gate Configuration



Z_i: The resistor R_S is directly across the terminals defining Z_i. Let us therefore find the impedance Z_i' which will simply be in parallel with R_S when Z_i is defined.



$$V' - V_{r_d} - V_{R_D} = 0$$

$$V_{r_d} = V' - V_{R_D} = V' - I'R_D$$

Applying Kirchhoff's current law at node a results in

$$I' + g_m V_{gs} = I_{r_d}$$

$$I' = I_{r_d} - g_m V_{gs} = \frac{(V' - I'R_D)}{r_d} - g_m V_{gs}$$

$$I' = \frac{V'}{r_d} - \frac{I'R_D}{r_d} - g_m[-V']$$

$$I'\left[1 + \frac{R_D}{r_d}\right] = V'\left[\frac{1}{r_d} + g_m\right]$$

$$Z_i' = \frac{V'}{I'} = \frac{\left[1 + \dfrac{R_D}{r_d}\right]}{\left[g_m + \dfrac{1}{r_d}\right]} = \frac{r_d + R_D}{1 + g_m r_d}$$

$$Z_i = R_S \| Z_i'$$

$$\boxed{Z_i = R_S \left\| \left[\frac{r_d + R_D}{1 + g_m r_d} \right] \right.}$$

If $r_d \geq 10R_D$, and $1/r_d \ll g_m$:

$$Z_i' = \frac{\left[1 + \dfrac{R_D}{r_d}\right]}{\left[g_m + \dfrac{1}{r_d}\right]} \cong \frac{1}{g_m}$$

$$\boxed{Z_i \cong R_S \| 1/g_m}_{r_d \geq 10R_D}$$

Z_o: Substituting $V_i = 0$ V in will "short-out" the effects of R_S and set V_{gs} to 0 V. The result is $g_m V_{gs} = 0$, and r_d will be in parallel with R_D. Therefore,

$$\boxed{Z_o = R_D \| r_d}$$

For $r_d \geq 10R_D$,

$$\boxed{Z_o \cong R_D}_{r_d \geq 10R_D}$$

A_v:

$$V_i = -V_{gs}$$

and

$$V_o = I_D R_D$$

The voltage across r_d is

$$V_{r_d} = V_o - V_i$$

and

$$I_{r_d} = \frac{V_o - V_i}{r_d}$$

Applying Kirchhoff's current law at node b results in

$$I_{r_d} + I_D + g_m V_{gs} = 0$$

and

$$I_D = -I_{rd} - g_m V_{gs}$$

$$= -\left[\frac{V_o - V_i}{r_d}\right] - g_m[-V_i]$$

$$I_D = \frac{V_i - V_o}{r_d} + g_m V_i$$

so that
$$V_o = I_D R_D = \left[\frac{V_i - V_o}{r_d} + g_m V_i\right] R_D$$
$$= \frac{V_i R_D}{r_d} - \frac{V_o R_D}{r_d} + g_m$$

and
$$V_o\left[1 + \frac{R_D}{r_d}\right] = V_i\left[\frac{R_D}{r_d} + g_m R_D\right]$$

with
$$A_v = \frac{V_o}{V_i} = \frac{\left[g_m R_D + \frac{R_D}{r_d}\right]}{\left[1 + \frac{R_D}{r_d}\right]}$$

For $r_d \geq 10R_D$,
$$A_v = g_m R_D \qquad r_d \geq 10R_D$$

Phase Relationship: The fact that A_v is a positive number will result in an *in-phase* relationship between V_o and V_i for the common-gate configuration.

Example 7

If $V_{GS_Q} = -2.2$ V and $I_{D_Q} = 2.03$ mA:

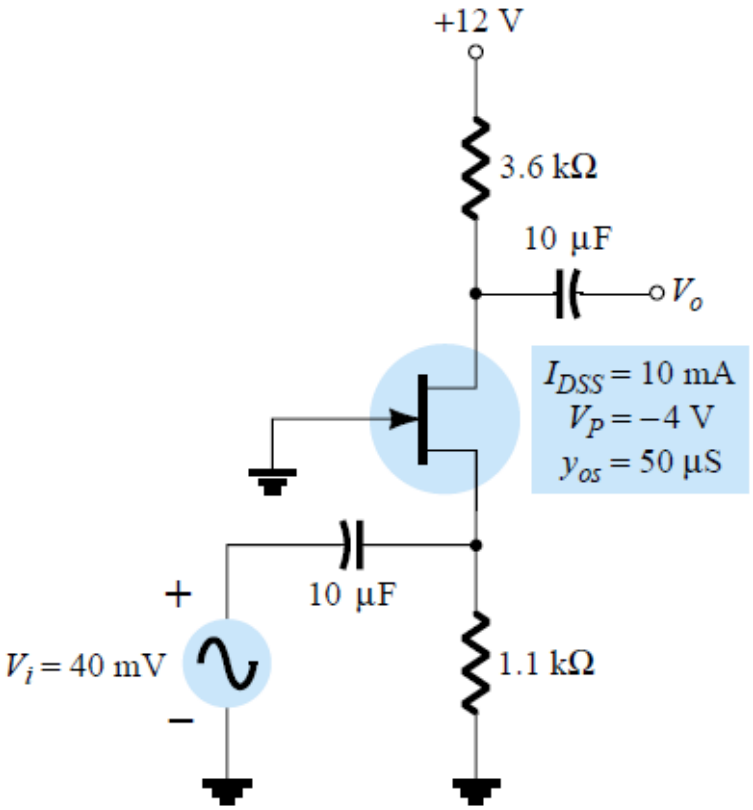
(a) Determine g_m.

(b) Find r_d.

(c) Calculate Z_i with and without r_d. Compare results.

(d) Find Z_o with and without r_d. Compare results.

(e) Determine V_o with and without r_d. Compare results.

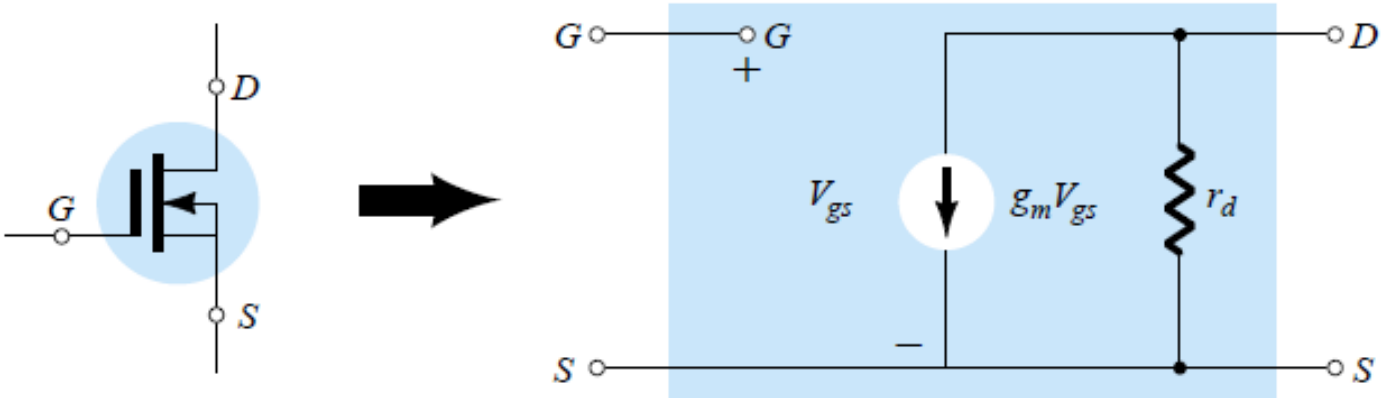


Solution

6. Depletion-Type MOSFETs Small Signal Model

The fact that Shockley's equation is also applicable to depletion-type MOSFETs results in the same equation for g_m. In fact, the ac equivalent model for D-MOSFETs is exactly the same as that employed for JFETs as shown in Fig. 9.33.

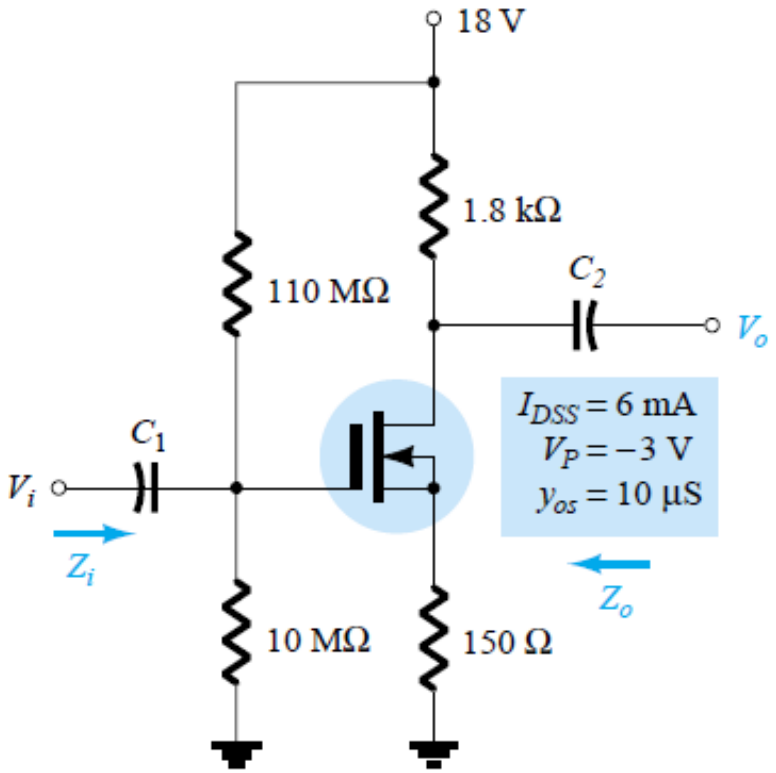
The only difference offered by D-MOSFETs is that V_{GSQ} can be positive for n-channel devices and negative for p-channel units. The result is that g_m can be greater than g_{m0} as demonstrated by the example to follow. The range of r_d is very similar to that encountered for JFETs.



Example 8

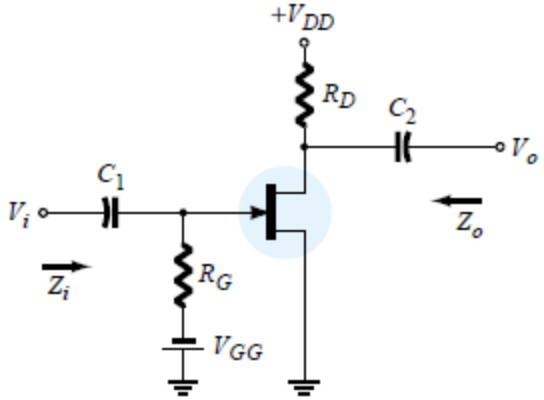
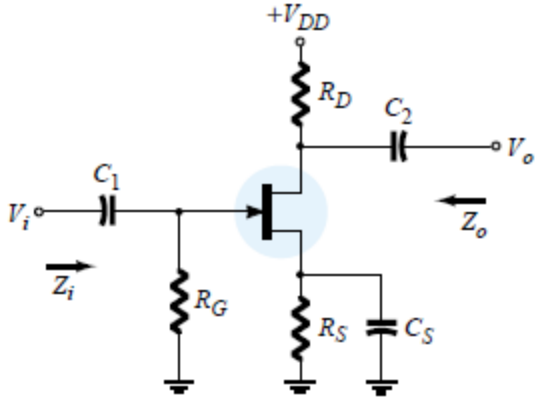
For the following circuit, if $V_{GS_Q} = 0.35$ V and $I_{D_Q} = 7.6$ mA.

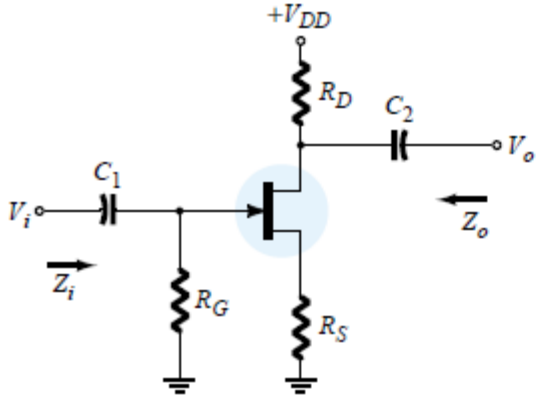
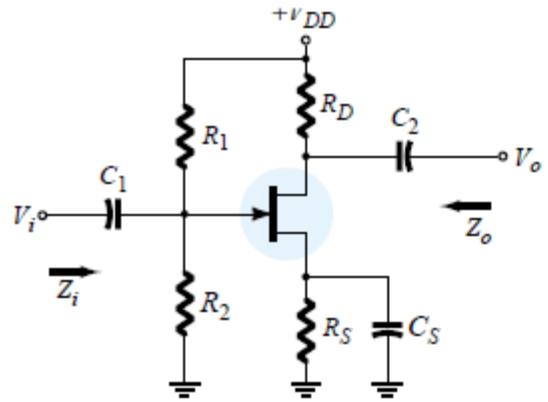
(a) Determine g_m and compare to g_{m0}.
(b) Find r_d.
(c) Sketch the ac equivalent network
(d) Find Z_i.
(e) Calculate Z_o.
(f) Find A_v.

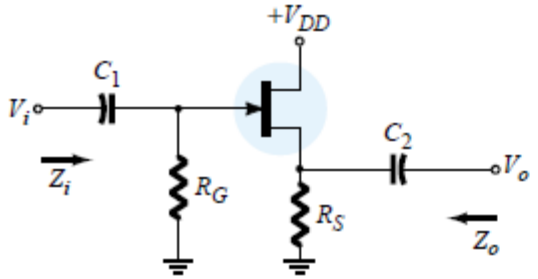
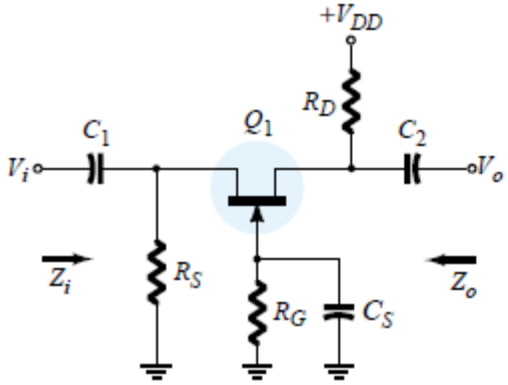


Solution

TABLE 9.1 Z_i, Z_0, and A_v for various FET configurations

Configuration	Z_i	Z_o	$A_v = \frac{V_o}{V_i}$
Fixed-bias [JFET or D-MOSFET]  	High (10 MΩ) $= R_G$	Medium (2 kΩ) $= R_D \| r_d$ $\cong R_D$ $(r_d \geq 10\,R_D)$	Medium (−10) $= -g_m(r_d \| R_D)$ $\cong -g_m R_D$ $(r_d \geq 10\,R_D)$
Self-bias bypassed R_s [JFET or D-MOSFET]  	High (10 MΩ) $= R_G$	Medium (2 kΩ) $= R_D \| r_d$ $\cong R_D$ $(r_d \geq 10\,R_D)$	Medium (−10) $= -g_m(r_d \| R_D)$ $\cong -g_m R_D$ $(r_d \geq 10\,R_D)$

Self-bias unbypassed R_S [JFET or D-MOSFET]  	High (10 MΩ) $= R_G$	$= \dfrac{\left[1 + g_m R_S + \dfrac{R_S}{r_d}\right] R_D}{\left[1 + g_m R_S + \dfrac{R_S}{r_d} + \dfrac{R_D}{r_d}\right]}$ $= R_D$ $r_d \geq 10\,R_D$ or $r_d = \infty\Omega$	Low (−2) $= \dfrac{g_m R_D}{1 + g_m R_s + \dfrac{R_D + R_S}{r_d}}$ $\cong -\dfrac{g_m R_D}{1 + g_m R_S}$ $[r_d \geq 10(R_d + R_S)]$
Voltage-divider bias [JFET or D-MOSFET]  	High (10 MΩ) $= R_1 \| R_2$	Medium (2 kΩ) $= R_D \| r$ $\cong R_D$ $(r_d \geq 10\,R_D)$	Medium (−10) $= -g_m(r_d \| R_D)$ $\cong -g_m R_D$ $(r_d \geq 10\,R_D)$

Configuration	Z_i	Z_o	$A_v = \frac{V_o}{V_i}$
Source-follower [JFET or D-MOSFET]  	High (10 MΩ) $= R_G$	Low (100 Ω) $= r_d \| R_S \| 1/g_m$ $\cong R_S \| 1/g_m \quad (r_d \geq 10\, R_S)$	Low (< 1) $= \frac{g_m(r_d \| R_S)}{1 + g_m(r_d \| R_S)}$ $\cong \frac{g_m R_S}{1 + g_m R_S} \quad (r_d \geq 10\, R_S)$
Common-gate [JFET or D-MOSFET]  	Low (1 kΩ) $= R_S \left\| \left[\frac{r_d + R_D}{1 + g_m r_d} \right] \right.$ $\cong R_S \left\| \frac{1}{g_m} \right. \quad (r_d \geq 10\, R_D)$	Medium (2 kΩ) $= R_D \| r_d$ $\cong R_D \quad (r_d \geq 10\, R_D)$	Medium (+10) $= \frac{g_m R_D + \frac{R_D}{r_d}}{1 + \frac{R_D}{r_d}}$ $\cong g_m R_D \quad (r_d \geq 10\, R_S)$